行政院國家科學委員會專題研究計畫 成果報告

可避免干擾雜訊的 SOC 晶片繞線系統的開發
研究成果報告(精簡版)

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行政院國家科學委員會補助專題研究計畫成果報告

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可避免干擾雜訊的 SOC 晶片繞線系統的開發

"Development of A Noise-Avoidance-Driven Routing System in SOC Chips"

計畫編號：NSC95-2221-E-216-058

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主持人：顏金泰 中華大學資訊工程系教授

一、中文摘要

對 SOC 晶片設計環境，此計劃希望發展可避免干擾雜訊的繞線系統達成繞線結果正確完整性，整個繞線系統大致分為以機率分析為基礎的干擾雜訊最少化的整體繞線、干擾雜訊降低之訊號線順序排列與時序導向軌線安排與最佳化隔離線的插入以符合干擾雜訊限制等三個主要部份。在機率分析為基礎的干擾雜訊最少化的整體繞線部份中，首先已知的電源供應系統共構的繞線模式，以機率分析方法計算可能跨過電源格線的機率，並利用電容與電感計算模式計算可能跨過電源格線的平均電容與電感值，進一步求得整體繞線結果機率式的平均干擾雜訊。依賴軟性連線與史丹爾端點移動的技巧，使得有效改良整體繞線結果，並藉由機率式的平均干擾雜訊做出干擾雜訊最少化的路徑設定，將可順利達成干擾雜訊最少化的整體繞線結果。進一步在干擾雜訊降低之訊號線順序排列與時序導向軌線安部份，依據所有跨過任一電源格線的連線資訊，設定連線最短距離幾何限制、連線交錯最少化限制、連線交錯分怖限制與訊號交互作用限制，利用拓樸排序方式完成干擾雜訊降低之訊號線順序排列。另一方面依據同列或同行電源格之訊號線順序排列，並且考量降低偶合電容所產生的額外延遲與降低電容感效應所產生的干擾雜訊，進一步執行線性規劃的設計達成干擾雜訊降低之時序導向軌線安排。最後在最佳化隔離線的插入以符合干擾雜訊限制部份，依據所有訊號線的干擾雜訊限制，尋找不符合干擾雜訊限制的訊號線，在同列或同行電源格上進一步利用較少的隔離線插入來完成最佳化隔離線的插入以符合干擾雜訊限制，使得晶片中所有訊號線都符合干擾雜訊限制，完成可避免干擾雜訊的繞線系統。

英文摘要

A noise-avoidance-driven routing system with signal integrity is developed for SOC design environment. Basically, the proposed system is divided into three phases: Probabilistic-based noise-minimization-driven global routing, Net ordering and timing-driven track routing for noise reduction and Optimal shielding insertion for noise constraints. In the noise-minimization-driven global routing phase, based on the codesign model of power and signal lines and the computation of probabilistic-based average crosstalk noise, the probabilistic-based congestion on all the power lines can be obtained. By using the concept of soft wiring and Steiner-point movement, the global routing result will be improved by reassigning all the Steiner points and routing paths to minimize the average crosstalk noise. Furthermore, according to the connection information on all the power grid lines, the geometrical distance constraint, the crossing minimization constraint, the crossing distribution constraint and the switching activity constraint are defined and the net ordering of all the signals in a power grid line is further obtained by using a topological sorting. Additionally, according to the net ordering of all the signals on all the power grid lines, the reduction of coupling delay and crosstalk noise is considered and timing-driven track routing in a row or column of grids is obtained by using a linear-programming-based approach. Finally,

based on the noise constraints of all the signal nets, the noise violation of all the signal nets can be released by optimally inserting a minimal set of shields in a row or column of grids. As a result, the noise violation of all the signal nets in a chip can be released to obtain a noise-avoidance-driven routing system.

二、計畫的緣由與目的

　　　隨著新世代製程技術的發展，使得整個系統建構於單晶片成為可能的事實，因此系統晶片(System-on-Chip，SOC) 的相關研究與技術受到產業界廣泛的注意，近來由於設計上的應用日漸複雜，SOC 晶片的設計往往涵蓋幾個主要部份，包括微處理器、DSP 處理器、記憶體、I/O、控制邏輯與混合訊號區塊等部份，利用各個功能模組化的 IP 技術開發，進而透過 IP 授權來達到設計得以重覆使用(IP Reuse)，使得獨立設計者也有能力整合 SOC 晶片來滿足市場上的需求，進而提昇系統應用的成效。

　　　但是新世代製程技術高電壓源(V_{dd})下降與 SOC 晶片上高密度的電路分佈，使得晶片中訊號連線彼此所產生的干擾雜訊(Crosstalk noise)日趨嚴重，倘若干擾雜訊的程度較輕微，可能影響電路上時序(Timing)延遲，導致晶片的效能降低，倘若干擾雜訊的程度較嚴重，可能進一步導致電路功能(function)正確性的失真。基本上對於干擾雜訊大部份取決於晶片繞線的結果，因此對於新世代製程技術下的 SOC 晶片而言，可避免干擾雜訊的繞線系統設計成為未來晶片成功的重要因素，因此訊號完整性(Signal Integrity)將是新一代晶片成功設計的一大課題。

　　　一般而言，對於發展可避免干擾雜訊的繞線系統，必須建立在精準的干擾雜訊評估模式與具有電源供應系統共構的繞線模式。對於現今新世代製程技術下的 SOC 晶片而言，晶片中的干擾雜訊來自於電路中的電容效應與電感效應，尤其電感效應在近代奈米技術中的雜訊影響所佔的比例日漸增高，因此準確的評估電路中電容與電感效應將是建立干擾雜訊模式重要的因素，進一步依據電子與電磁理論計算感應產生的干擾雜訊量。另一方面隨著晶片連線的日趨複雜，為了對於大量連線磁場效應所產生干擾雜訊有效控制，通常在避免干擾雜

訊的繞線系統上使用具有電源供應系統共構的繞線模式，如圖一所示，首先新世代製程技術下的 SOC 晶片可能以電源格狀(Power Grid)連線的拓璞結構的方式[1-2]來提供所有元件有效的供電，電源格狀連線中的所有格狀區域將提供所有訊號線繞線連接使用，藉由電源連線隔離不同格狀區域內的電感磁場，使得不同格狀區域內的訊號線不產生干擾雜訊，讓大量干擾雜訊的累加現象得到有效的控制[3]，因此發展可避免干擾雜訊的繞線系統需仰賴電源供應系統連線的結果。基於精準的干擾雜訊評估模式與具有電源供應系統共構的繞線模式的條件，可避免干擾雜訊的繞線系統通常分成下列四個方向分別探討並整合完成：干擾雜訊模式與可容許雜訊限制、以干擾雜訊最少為目標的整體繞線、訊號線順序排列與軌線安排與隔離線的插入以減少干擾雜訊。
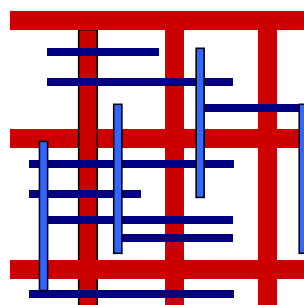

圖一　電源供應系統共構的繞線模式

三、研究方法及成果

　　　此計劃希望針對 SOC 晶片設計環境，發展可避免干擾雜訊的繞線系統達成繞線結果訊號正確完整性，基於晶片中任一訊號線干擾雜訊的計算方式與具有電源供應系統共構的繞線模式，整個繞線系統大致分為以機率分析為基礎的干擾雜訊最少化的整體繞線、干擾雜訊降低之訊號線順序排列與時序導向軌線安排與最佳化隔離線的插入以符合干擾雜訊限制等三個主要部份。

A. 以機率分析為基礎的干擾雜訊最少化的整體繞線

　　　針對已知的電源供應系統共構的繞線模式，為了完成干擾雜訊最少化的整體繞線，必需在整體繞線階段評估晶片中任何訊號線的干擾雜訊，一般而言，任何訊號線的干擾雜訊必需等到繞線確定完成才可計算得知，因此在

整體繞線階段必需以機率分析方式計算任何訊號線的平均干擾雜訊為完成干擾雜訊最少化整體繞線的目標。基本上對於任何訊號線的平均干擾雜訊，以機率分析方法計算可能跨過電源格線的機率，並且以機率分析方法計算在電源格線上平均干擾係數，進一步利用電容與電感計算模式計算可能跨過電源格線的平均電容與電感值，求得整體繞線結果上機率式的平均干擾雜訊。對於任一連線可能跨過電源格線的機率，首先考慮此連線的最小繞線面積，並求出被最小繞線面積包含的所有電源格線，根據所有可能繞線數目與行經某電源格線所有可能繞線數目，以機率平均分佈的概念算出此連線跨過某電源格線的機率。另一方面如圖二所示，對於電源格線上平均干擾係數，根據 Prof. He 所提出線性計算模式，容易依照連線在電源格線的位置，計算相對應的干擾係數，既然整體繞線結果沒有連線在電源格線的正確位置，只能以機率平均分佈的概念計算出連線在電源格線的平均干擾係數。一旦所有電源格線得連現都算出可能跨過電源格線的機率和連線在電源格線的平均干擾係數，依據所有繞線樹分佈與線段長度資訊，很容易計算出所有繞線樹的平均干擾雜訊。


圖二　線性干擾係數計算模式
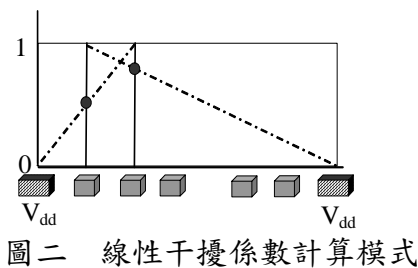
一般而言每個繞線樹可能擁有由史丹爾端點構成的 Y 型連線，既然史丹爾端點先天有可移動的特性，藉由史丹爾端點移動可改變樹形路徑，不破壞原來延遲限制條件之下，即可將每個史丹爾端點的可移動區域求得，這個史丹爾端點的可移動區域的定義也將使得繞線樹有足夠的繞線彈性，進而達成平衡擁擠現象下用來減少平均干擾雜訊。基本上整體繞線結果會影響跨過電源格線的平均干擾雜訊，全晶片干擾雜訊最少化的整體繞線結果建立在如何不破壞原來延遲限制條件之下，利用計算出的所有電源格線上平均干擾雜訊，適當的依賴軟性連線與史丹爾端點移動的技巧來改變每

個繞線樹的路徑，並配合延遲條件的計算，將每個史丹爾端點的可移動區域求得，進一步依照相關電源格線的位置，即可藉由史丹爾端點移動的技巧來調整相關電源格線的擁擠現象，並有效減少整體繞線結果的平均干擾雜訊和達成全晶片可繞性的整體繞線規劃。

B. 干擾雜訊降低之訊號線順序排列與時序導向軌線安排

　　考慮此電源格線上訊號線的順序排列時，首先得依據連線最短距離幾何、連線所有連線交錯關係與訊號交互作用資訊定義下列四個順序排列限制。隨著最短距離限制、連線交錯分佈限制與訊號交互作用限制的設定，將可建立相關符合順序排列的圖形結構，進一步利用圖形理論上拓樸排序方式完成此電源格線上干擾雜訊降低之訊號線順序排列。

　　當所有電源格線上之訊號線可能順序排列已求得，已知同列或同行電源格可跨越訊號線之容量，可慮同列或同行電源格之訊號線可能順序排列，依據相同訊號線在同列或同行電源格上排列不產生額外分支的合理性、考量降低偶合電容所產生的額外延遲與降低電容感效應所產生的干擾雜訊，進一步規劃線性方程式限制，以時序導向並降低所有干擾雜訊為目標，執行線性規劃程式尋求最佳的的軌線安排，以達成干擾雜訊降低之時序導向軌線安排設計。如圖三所示，倘若電源格線之容量為6，同行電源格由上而下之之訊號線順序排列為(4, 3, 6, 2, 7, 1)，(3, 8, 2, 1)，(5, 3, 8, 9, 1)和(8, 9, 1)，藉由降低所有干擾雜訊為目標，最佳的的軌線安排將可求得。
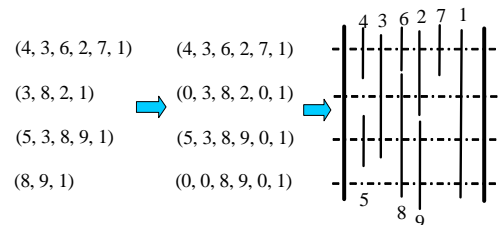
圖三　干擾雜訊降低之時序導向軌線安排

C. 最佳化隔離線的插入以符合干擾雜訊限制

　　當所有電源格線上之干擾雜訊降低之時序導向軌線安排已求得，依據訊號線干擾雜訊的計算模式與所有訊號線的干擾雜訊限制，尋

找不符合干擾雜訊限制的訊號線，考量具有不符合限制訊號線的同列或同行電源格，一般任一不符合限制訊號線至多只需差入兩條隔離線即可解除干擾雜訊限制，倘若依據此不符合限制訊號線位置找出可用來插入隔離線的範圍區，則每個不符合限制訊號線只有四種不符干擾雜訊限制的情況，在同行電源格中，此不符合限制訊號線算出一個它的可用來插入隔離線的範圍區，並且插入一條隔離線即可解除干擾雜訊限制，在同行電源格中，此不符合限制訊號線算出兩個它的可用來插入隔離線的範圍區，並且必需訊號線兩邊各插入一條隔離線才能解除干擾雜訊限制。

　　對於最佳化隔離線的插入以符合干擾雜訊限制，考量具有不符合限制訊號線的同列或同行電源格，所有不符合限制訊號線的可用來插入隔離線的範圍區都已求得，針對同列或同行電源格中由左而右或由上而下尋找最佳插入隔離線的位置。在同行電源格中，對於最左一條不符合限制訊號線而言，四種不符干擾雜訊限制的情況使得可能立刻決定一條必要隔離線的最佳插入位置或建構出訊號線關鍵插入範圍區。

　　當初始的訊號線關鍵插入範圍區建構完成，繼續考量下一條不符合限制訊號線，針對它的四種不符干擾雜訊限制的情況與關鍵插入範圍區的區域幾何交集現象，下一條必要隔離線的最佳插入位置也將可立刻決定。新的訊號線關鍵插入範圍區隨即更新，進一步利用遞迴程序處理下一條不符合限制訊號線、決定下一條必要隔離線的最佳插入位置與訊號線關鍵插入範圍區隨即更新，直到所有不符合限制訊號線處理完畢為止。既然所有隔離線的插入位置都是必要的最佳位置，利用較少的隔離線插入來完成最佳化隔離線的插入以符合干擾雜訊限制，使得晶片中所有訊號線都符合干擾雜訊限制，完成可避免干擾雜訊的繞線系統。

四、結論與討論

　　本計畫基於晶片中任一訊號線干擾雜訊的計算方式與具有電源供應系統共構的繞線模式，提出新的可避免干擾雜訊的繞線系統達成繞線結果訊號正確完整性，這樣的研究盼望對於新世代製程環境中高運算頻率 SOC 晶片

的電源共構的繞線系統提出有效的解決方法。本研究群的相關研究結果發表於 IEEE 會議論文 2 篇，並有一篇期刊論文與一篇 IEEE 會議論文已經投稿中。

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行政院國家科學委員會補助國內專家學者出席國際學術會議報告

報告人姓名	顏金泰	服務機構 及職稱	資訊工程學系 副教授
會議時間 會議地點	95/12/10-95/12/13 法國尼斯	本會核定 補助文號	
會議名稱	（中文）2006 年度國際電機電子工程師協會國際電子、電路與系統會議 （英文）2006 International Conference on Electronics, Circuits and Systems		
發表論文題目	（中文）基於機率式端點連接分析的良率導向多於端點插入設計 （英文）Yield-Driven Redundant Via Insertion Based on Probabilistic Via-Connection Analysis （中文）對於細部版面設計執行面積導向的空白空間分配 （英文）Area-Driven White Space Distribution for Detailed Floorplan Design		

報告內容應包括下列各項：

一、參加會議經過

12/10 由桃園國際機場搭中華航空經香港轉法國航空 AF182 班機抵達法國巴黎戴高樂機場，12/11 轉接法國高速鐵路抵達尼斯完成會議報到。12/12 下午前往會場參與 System Integration II Section 論文發表會並發表論文。12/13 前往會場參與 System Integration Section 論文發表會並發表論文。12/14 轉接法國高速鐵路由尼斯回抵巴黎。12/18 由法國巴黎戴高樂機場搭法國航空 AF183 經香港轉機抵達桃園國際機場。

二、與會心得

ICECS 是歐洲地中海區域最主要的電子、電路與系統會議，今年許多亞洲 Circuits 與 Systems 的研究發表此會議並且取得此會議最佳論文獎，可見亞洲電子系統發展能力受到世界的注目，台灣電子工業的發展須由造為導向轉型研究為導向來發展，才能在電子產業開創新的局面，因此投入電子電路與系統的研究發展應為灣電子業轉型的關鍵。

三、考察參觀活動(無是項活動者省略)
無

四、建議

國內大學研究團隊參與此次國際學術研討活動甚為積極，政府單位應多補助經費鼓勵大學研究成果多多發表國際學術研討會，以提升國內研究成果。

五、攜回資料名稱及內容
ICECS2006 論文集光碟片一片

六、其他

Yield-Driven Redundant Via Insertion Based on Probabilistic Via-Connection Analysis

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Abstract -- **In this paper, based on probabilistic via-connection analysis of single vias and redundant vias, it is well known that on-track redundant via insertion is more important and critical than off-track redundant via insertion for yield optimization. Furthermore, a two-phase insertion approach for yield optimization is proposed to insert on-track redundant vias by finding a maximum matching result in a bipartite graph and insert off-track redundant vias by using a maximum constrained edge-pair matching result in a multi-partite graph with via-sharing constraints. According to the Poisson yield model for redundant via insertion, the experimental results show that our proposed two-phase insertion approach can increase 0.3%~7.4% wirelength to improve 4.3%~44.8% chip yield for the tested benchmarks.**

I. INTRODUCTION

Due to the difficulty of lithography and manufacture in nanometer process, the concept of yield-driven design becomes more and more important for modern chip designs[1]. Basically, many physical factors will lead to the yield loss in a complete chip. For a given design, the design flow may focus on the yield impact on three physical factors: wires, vias and cells. To reduce the yield loss due to via failures is one of the most important issues in DFM. In general, the concept of redundant via insertion for yield improvement is applied in the routing or post-routing stage. Firstly, Allan and Walton[2-3] have proposed the techniques of redundant via placement to increase yield and reliability. Besides that, the commercial tools[4], EYE/PEYE, have inserted redundant vias to reduce the yield loss in the post-routing stage.

Recently, several researches[5-6] consider redundant via insertion for yield improvement in the routing stage. Xu et al.[5] propose a Lagrangian relaxation approach to insert on-track and off-track vias and Yao et al.[6] consider the via minimization to insert redundant vias in an existing multi-level routing framework. However, post-routing ECO operations may modify the final routing result and introduce the extra vias to fix the timing or antenna purpose. Hence, it is necessary for the yield and reliability to further perform redundant via insertion in the post-routing stage. On the other hand, several researches[7] consider redundant via insertion for yield improvement in the post-routing stage. Lee et al[7] reduce the redundant via insertion problem into the maximum independent set(MIS) problem and all single

vias in a routing result are simultaneously considered to insert on-track or off-track vias by using the MIS-based approach with effective heuristics. However, the MIS-based approach takes more execution time to insert on-track or off-track vias for yield improvement. Beside that, all the single vias in a routing result in Luo's approach[8], are considered one by one to perform the redundant via insertion. Since the approach changes the routing result of the non-critical nets, it may induce the timing violation even if the critical time is kept unchanged. However, the final solutions may be locally optimal for yield optimization.

In this paper, based on probabilistic via-connection analysis of single vias and redundant vias, it is well known that on-track redundant via insertion is more important and critical than off-track redundant via insertion for yield optimization. Furthermore, a two-phase insertion approach for yield optimization is proposed to insert on-track redundant vias by finding a maximum matching result in a bipartite graph and insert off-track redundant vias by using a maximum constrained edge-pair matching result in a multi-partite graph with via-sharing constraints. According to the Poisson yield model for redundant via insertion, the experimental results show that our proposed two-phase insertion approach can increase 0.5%~7.0% wirelength to improve 4.3%~44.8% chip yield for the tested benchmarks.

II. PROBLEM FORMULATION

Basically, any via in an IC layout provides the connection of wire segments between two adjacent metal layers. Due to various manufacturing reasons, the connecting vias may fail partially or completely. For a partial-failed via, the connecting resistance will increase to cause unexpected delay. On the other hand, a complete-failed via will lead to the functionality invalidation in the design.

Given a detailed routing result with n signal nets, all the wire segments for net i are connected by using m_i single vias between two adjacent layers. For the connection of any via between two wire segments, it is assumed that any of the two wire segments is fully connected. As the connecting probability of the j-th via in net i is defined as P_j^i, the failure probability, λ_i, for net i can be obtained as $1 - \prod_{j=1}^{m_i} P_j^i$ due to the

via failure. Furthermore, the chip yield, Y_v, based on the

Poisson model [3] can be defined as $\prod_{i=1}^{n} e^{-\lambda_i}$, due to the via failure, that is,

$$Y_v = \prod_{i=1}^{n} e^{-\lambda_i} \cdot$$

Generally speaking, the yield loss of any via in an IC layout can be reduced by adding a redundant via adjacent to the original via without violating any design rule. The redundant vias can be divided into on-track and off-track redundant vias. Basically, an on-track redundant via can be constructed by adding an extra inner wire segment to connect the original via. On the other hand, an off-track redundant via can be constructed by adding two extra outer wire segments to connect the original via. As shown in Fig. 1(a), the top view and the 3D structure of a single via connecting two wire segments are illustrated. Furthermore, the top view and the 3D structure of a single via and its redundant via after adding an on-track or off-track redundant via are illustrated in Fig. 1(b) and Fig. 1(c), respectively.
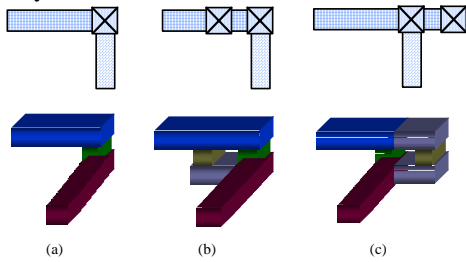

(a)　　　　(b)　　　　(c)

Fig. 1 Top view and 3D structure of a single via and on-track and off-track redundant vias

Given a detailed routing result without re-routing any signal net, the yield-driven redundant via insertion(YRVI) problem is to maximize the chip yield due to the via failure by inserting redundant vias into single vias on signal nets subject to the following condition: each single via either remains unchanged or inserts a redundant via without violating any design rule. As shown in Fig. 2(a), given a detailed routing result in 4 layers, the final detailed routing result as shown in Fig. 2(b) can be obtained to improve the chip yield by inserting on-track and off-track redundant vias.
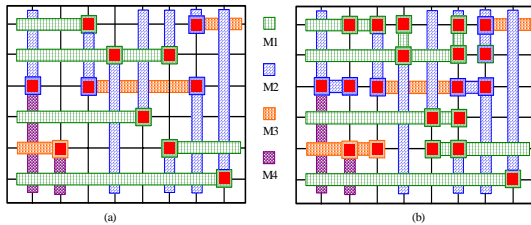

(a)　　　　　　　　(b)

Fig. 2 Redundant via insertion for yield optimization

III. TWO-PHASE APPROACH FOR REDUNDANT VIA INSERTION

Basically, the concept of redundant via insertion can be used to reduce the yield loss due to via failure. Based on the connection analysis of any single via and its redundant via,

it is well known that on-track redundant via insertion is more important and critical that off-track redundant via insertion for yield optimization. Hence, a two-phase insertion approach for yield optimization is proposed to insert yield-driven on-track and off-track redundant vias, respectively.

3.1 Probabilistic Connection Analysis for Redundant Vias

For the connection analysis of any single via and its redundant via, it is initially assumed that any of two wire segments connected by the original via is fully connected. If the failure probability of a single via is defined as p_v , the connecting probability, P_0 , of the single via can be obtained as $(1 - p_v)$, that is,

$$P_0 = (1 - p_v) \cdot$$

As an on-track redundant via and an extra inner wire segment are added to connect two wire segments, the connecting probability, $P_{1,on}$, of the single via and its on-track redundant via can be obtained as $(1 - p_v) + p_v(1 - p_v)(1 - p_e)$, that is,

$$P_{1,on} = (1 - p_v) + p_v(1 - p_v)(1 - p_e) ,$$

if the failure probability of the extra segment is further defined as p_e .

On the other hand, As an off-track redundant via and two extra outer wire segments are added to connect two wire segments, the connecting probability, $P_{1,off}$, of the single via and its off-track redundant via can be obtained as $(1 - p_v) + p_v(1 - p_v)(1 - p_e)^2$, that is,

$$P_{1,off} = (1 - p_v) + p_v(1 - p_v)(1 - p_e)^2 \cdot$$

According to the fact that the values of the probabilities, p_v and p_e in P_0 , $P_{1,on}$ and $P_{1,off}$, are both less than 1, Clearly, the value of the connecting probability, $P_{1,on}$, is always larger than that of the connecting probability, $P_{1,off}$, and the value of the connecting probability, $P_{1,off}$, is always larger than that of the connecting probability, P_0 . For the chip yield, the connecting probability of the j-th via in net i , P_j^i , is only P_0 , $P_{1,on}$ or $P_{1,off}$. Based on the probabilistic via-connection analysis, the concept of redundant via insertion can be guaranteed to reduce the via-connection failure for yield optimization. Besides that, it is well known that on-track redundant via insertion is more important and critical than off-track redundant via insertion for yield optimization.

3.2 Yield-driven On-track Redundant Via Insertion

For yield-driven on-track redundant via insertion, all the redundant vias are adjacent to the single vias and added onto the tracks of the signal nets. Hence, the insertion of on-track redundant vias on the signal nets is independent each other. For a single via, the adjacent location permitting to insert an

on-track via is called as a valid on-track location according to the given detailed routing result and the design rule. As two single vias are not on the same layer and have a common valid on-track location, the valid location must be treated as two different locations. As shown in Fig. 3, two on-track redundant vias can be simultaneously added onto a common valid location for two single vias.
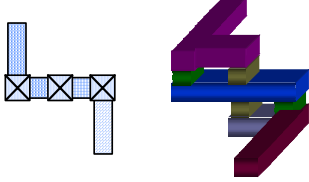

Fig. 3 On-track redundant vias on the same location

For any signal net, N_i, in an IC layout, a corresponding bipartite graph, $G_i(V, E)$, can be constructed to further find all the locations of on-track redundant vias. Basically, the vertex set, V, in G_i can be divided into the via-vertex set, V_V, and the location-vertex set, V_L. Each vertex in V_V represents a single via in N_i and each vertex in V_L represents a valid on-track location of any single via. As two single vias are not on the same layer and have a common valid on-track location, the location vertex must be duplicated. Each edge between V_V and V_L represents any single via in V_V may add an on-track redundant via onto its valid location in V_L. According to the construction of a bipartite graph for any signal net, N_i, the yield-driven on-track redundant via insertion can be obtained to insert as many redundant vias as possible by finding a maximum matching result in G_i. Given the detailed routing result in Fig. 4(a), the single vias in only two signal nets have valid on-track locations. Hence, two corresponding bipartite graphs in Fig. 4(b) can be constructed to find a maximum matching result.
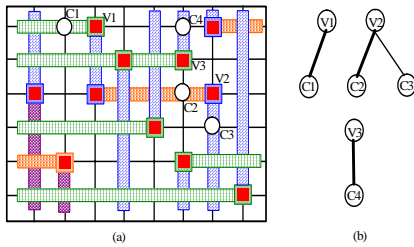

Fig. 4 Yield-driven on-track redundant via insertion

For any bipartite graph, $G_i(V, E)$, an on-track redundant via can be represented as an edge between V_L and V_V. According to the construction of a bipartite graph, it is clear that the degree of each vertex in V is at most 4. An optimal iterative approach can be proposed to find a maximum matching result as follows: First, any location vertex with the minimum degree and its connecting via vertex are selected as a matching pair. After selecting a matching pair, the corresponding vertices and edge in the bipartite graph will be deleted. Until no location vertex is found, the process will stop and the final maximum matching result will be obtained. Clearly, the complexity of yield-driven on-

track redundant via insertion is in O(n) in the worst case, where n is the number of single vias in an IC layout. As illustrated in Fig. 4, 3 on-track redundant vias, V1, V2 and V3, are added onto the valid locations, C1, C2 and C4, to improve the chip yield for yield-driven on-track redundant via insertion.

3.3 Yield-driven Off-track Redundant Via Insertion

For yield-driven off-track redundant via insertion, all the redundant vias are adjacent to the single vias and added onto the extended wire segments of the single vias. For a single via, the adjacent location permitting to insert an off-track via is called as a valid off-track location according to the given detailed routing result and the design rule. It is possible that several single vias have a common valid off-track location for off-track redundant via insertion. Hence, the off-track redundant via insertion of all the signal nets must be considered at the same time.

For the single vias on all the signal nets, a corresponding multi-partite graph, $G(V, E)$, with the constraint set, C, can be constructed to further find the locations of the off-track redundant vias for all the signal nets. Basically, the vertex set, V, in G can be divided into several via-vertex sets, $V_{V,1}$, $V_{V,2} \ldots V_{V,m}$, and several location-vertex sets, $V_{L,1}$, $V_{L,2} \ldots V_{L,m+1}$, according to the layer location of all the vias. Each vertex in $V_{V,i}$ represents a single via on the i-th via layer and each vertex in $V_{L,j}$ represents a valid off-track location of any single via on on the j-th metal layer. The pair of one edge between $V_{L,i}$ and $V_{V,i}$ and the other edge between $V_{V,i}$ and $V_{L,i+1}$ in E represents any single via in $V_{V,i}$ may add an off-track redundant via onto the same valid location in $V_{L,i}$ and $V_{L,i+1}$.

As two single vias in the same signal net form stacked vias and have at least one common valid off-track location, the valid location can be shared by the two stacked vias. Basically, the stacked sharing phenomenon can be defined as a *via-sharing constraint*, and any constraint in C is a via-sharing constraint. As shown in Fig. 5, two single vias form stacked vias and two off-track redundant vias can be simultaneously added onto a common valid location for the two stacked vias.
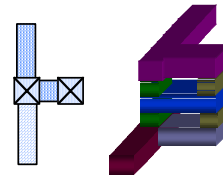

Fig. 5 Off-track redundant vias on the same location

According to the construction of a multi-partite graph and the via-sharing constraint for all the signal nets, the yield-driven off-track redundant via insertion can be obtained to insert as many redundant vias as possible by finding a maximum constrained edge-pair matching in G. As shown in Fig. 6(a), 3 on-track redundant vias are added into the detailed routing result. According to the positions of 8

single vias, V4, V5…V11, and 6 valid off-track locations, C5, C6,…, C10, on different layers and a via-sharing constraint on C5, a corresponding multi-partite graph in Fig. 6(b) can be constructed to find a maximum constrained edge-pair matching result.
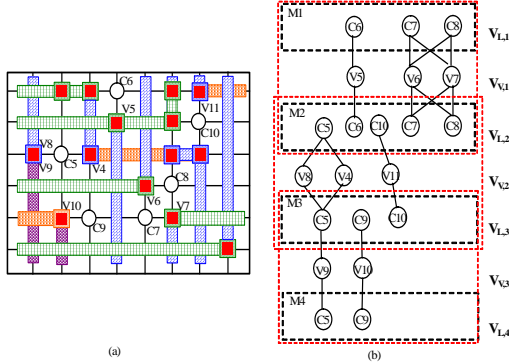

Fig. 6 Yield-driven off-track redundant via insertion

Basically, an off-track redundant via is used to connect the same location on two adjacent layers. For a multi-partite graph, $G(V, E)$, with via-sharing constraints, C, an off-track redundant via can be represented by the pair of one edge between $V_{L,i}$ and $V_{V,i}$ and the other edge between $V_{V,i}$ and $V_{L,i+1}$ in E. Hence, a multi-partite graph can be treated as several overlapped pair stages for the edge-pair matching search. In Fig. 6(b), the multi-partite graph can be treated as 3 overlapped pair stages illustrated by dotted boxes.

According to the construction of a multi-partite graph, it is clear that the degree of each via-vertex in V is at most 4 and the degree of each location-vertex in V is at most 8. An optimal iterative approach can be proposed to find maximum constrained edge-pair matching result in the overlapped pair stages as follows: First, any location vertex with the minimum degree in the overlapped pair stages is found and the same location vertex on two adjacent layers and its connecting via vertex are selected as an edge-pair matching. If the edge-pair matching is involved in a via-sharing constraint, the other sharing edge-pair matching can be further obtained according to the position of the location vertex. After selecting edge-pair matching, the corresponding vertices and edge in the multi-partite graph will be deleted. Until no location vertex is found, the process will stop and the final maximum edge-pair matching result will be obtained. Clearly, the complexity of yield-driven off-track redundant via insertion is in O(n) in the worst case, where n is the number of single vias in an IC layout. As a result, 5 off-track redundant vias, V5, V6, V7, V10 and V11, are added onto the valid locations, C6, C7, C8, C9 and C10, and 2 off-track redundant vias are added and shared onto the valid locations, C5, to improve the chip yield for yield-driven off-track redundant via insertion.

IV. EXPERIMENTAL RESULTS

For the YRVI problem, our proposed two-phase insertion approach has been implemented by using standard C++

language and run on a Pentium IV 2.8GHz machine. 11 detailed routing results, Mcc1, Mcc2, Primary1, Primary2, Struct, S5378, S9234, S13207, S15850, S38417 and S38584, have been applied to test the yield improvement in the proposed two-phase approach for yield-driven redundant via insertion. In the experiment, the failure probabilities, p_v and p_e, are set as 0.00001 and 0.000001. The experimental results have been shown in Table I. According to the Poisson yield model for redundant via insertion, the experimental results show that our proposed two-phase insertion approach can increase 0.3%~7.4% wirelength to improve 4.3%~44.8% chip yield for the tested benchmarks.

TABLE I EXPERIMENTAL RESULTS FOR YIELD-DRIVEN REDUNDANT VIA INSERTION

Circuits	Original			Two-Phase redundant Via Insertion		
	WireLength	#Via	Yield	Length	#RedundantVia	Yield
Mcc1	28204910000	4462	0.956367	28433710000	4222(4222+0)	0.999999
Mcc2	405992754000	25940	0.771517	407361704000	25172(25172+0)	0.999997
Promary1	1032261500	4489	0.956105	1037547500	4309(4309+0)	0.999999
Primary2	4203679000	18231	0.833357	4224891400	17345(17345+0)	0.999998
Struct	862096400	6780	0.934450	870311600	6560(6560+0)	0.999999
S5378	75547230	6866	0.933648	80484270	6614(6541+39)	0.999269
S9234	56118920	5757	0.944059	60251000	5531(5498+27)	0.999879
S13207	179278838	14923	0.861384	189992438	14419(14324+62)	0.999668
S15850	222493218	17875	0.836335	235323618	17243(17119+87)	0.999628
S38417	486579940	44048	0.643864	518220340	42569(42260+226)	0.999165
S38584	675813009	59646	0.551400	718779729	57599(57194+327)	0.999214

V. CONCLUSIONS

The yield loss of any via in an IC layout can be reduced by adding a redundant via adjacent to the original via without violating any design rule. A two-phase insertion approach is proposed for yield optimization based on probabilistic via-connection analysis of redundant vias.

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Area-Driven White Space Distribution for Detailed Floorplan Design

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Abstract --In this paper, based on the LB-packing-based property in an LB-compact floorplan, some white space for advanced design requirement is considered. By using the grouping concept of the block and the necessary space, the white space in a floorplan is redistributed to minimize the final floorplan area with satisfying all the space requirements. After running our proposed area-driven white space distribution, the experimental results show that the area increase is 1.4%~7.2% based on 4.2%~11.2% space requirement for the tested benchmarks in reasonable time. Clearly, the proposed LB-packing-based approach can redistribute the original white space to satisfy most of the space requirements.

I. INTRODUCTION

As the concept of deep sub-micron fabrication technology makes billion-transistor chips to be a reality, floorplan design has become one of the most challenging tasks in VLSI circuit layout. As more and more components are placed on a VLSI chip, it is practically impossible for the most experienced circuit designers to optimally arrange all the components manually without using any automation tool. With rapidly narrowing interconnects in VLSI chips, floorplan design[1-2] also becomes a critical phase in timing-driven consideration.

Recently, the concept of high-speed and low-power designs leads to the development of modern VLSI circuits. In order to complete a high-speed or lower-power design, several extra logic gates must be introduced into the original circuit network. For example, the delay of the critical interconnection in any timing-driven design can be reduced by inserting buffers into feasible position[3]. Even for a pipelined design, the critical interconnection must be partitioned by inserting feasible flip-flops[4] because the interconnection delay becomes the main factor of the circuit delay. For a low-power design, the clock system may be constructed into a gating-clock structure by inserting AND gates[5], or the power system may be modified into a dual-voltage system by inserting necessary level-converters[6]. Besides that, the signal integrity problem in modern VLSI designs has become more important. In order to maintain the signal integrity, several necessary decoupling capacitance must be introduced and arranged into the original floorplan[7-8]. Basically, these inserted devices or gates must occupy some floorplan area. Hence, some white space in a floorplan plane must be further reserved to achieve advanced design requirement.

In general, the space requirement is not considered in the traditional placement/floorplan problem. Currently, the issue of white space allocation is studied and considered in standard-cell placement. Routability-driven white space allocation[9-10] has been developed to improve the routability of a complicated chip. Besides that, the white space requirement is further considered as a placement constraint[11] for mixed-size placement. In a block-level floorplanning result, the redistribution of white space[12] can be applied to minimize total wire length.

In this paper, based on the LB-packing-based property in an LB-compact floorplan, some white space for advanced design requirement is considered. By using the grouping concept of the block and the necessary space, the white space in a floorplan is redistributed to minimize the final floorplan area with satisfying all the space requirements. After running our proposed area-driven white space distribution, the experimental results show that the area increase is 1.4%~7.2% based on 4.2%~11.2% space requirement for the tested benchmarks in reasonable time. Clearly, the proposed LB-packing-based approach can redistribute the original white space to satisfy most of the space requirements.

II. PROBLEM FORMULATION

It is well known that feasible white space in a floorplan plane is applied to not only introduces the buffer insertion to speed up the interconnect delay but also arranges necessary decoupling capacitance to maintain the signal integrity. However, most of the floorplans do not consider the space distribution between any pair of adjacent blocks for advanced design requirement. For any LB(Left-Bottom)-compact floorplan, the space requirement between any pair of adjacent blocks can be easily estimated according to the layout area of logic gates for different design purposes. In general, the space requirement can be satisfied by horizontally or vertically shifting any of two adjacent blocks. Basically, the required space between two adjacent blocks must be simultaneously adjacent to two adjacent blocks. As shown in Fig. 1, the required space between the blocks, B_i and B_j, is introduced by inserting a horizontal or vertical space.
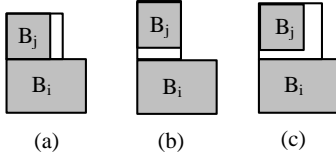
Fig. 1 Reasonable arrangement for space requirement

For any LB-compact floorplan with the space requirement, the white space distribution may increase the final floorplan area. Hence, the area-driven white space distribution problem is to use minimum extra area to satisfy all the space requirements by horizontally or vertically shifting some blocks in the floorplan. In Fig. 2, a final floorplan with satisfying all the space requirements is obtained by doing area-driven white space distribution for an LB-compact floorplan.
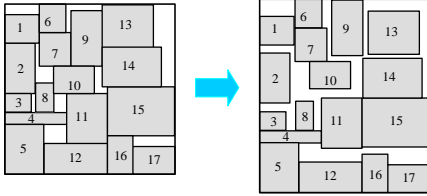

Fig. 2 Area-driven space distribution for detailed floorplan design

III. UNPACKING TRANSFORMATION IN AN LB-COMPACT FLOORPLAN

Given any pair of two blocks, B_i and B_j, in an LB-compact floorplan, F, there exists a horizontal(vertical) adjacent relation, $B_i \rightarrow B_j$, between blocks, B_i and B_j if B_i is horizontally(vertically) physically adjacent to B_j, or B_i moves horizontally to its right(vertically upward) to be physically adjacent to B_j without moving any other block. It is assumed that four rectangular boundaries, L, R, T and B, are treated as four dummy blocks in an LB-compacted floorplan, F. As a result, the horizontal(vertical) adjacent graph G_H (V_F, E_F) (G_V (V_F, E_F)) in F can be constructed by using all the horizontal(vertical) adjacent relations with the block widths as the edge weights in F, where V_F is the union of the block set in F and the set {L, R}({T, B}), and E_F is the set of all the horizontal(vertical) adjacent relations in V_F, respectively. Clearly, the floorplan width(height) can be obtained by finding the length of the longest path in the horizontal(vertical) adjacent graph. Furthermore, the floorplan area can be obtained by multiplying the floorplan width by the floorplan height. It is known that the circuit blocks called as *horizontal(vertical) critical blocks* in the horizontal (vertical) longest paths are not horizontally(vertically) movable if the floorplan width(height) is fixed. In contrast, if any circuit block is not located inside any of the longest path in the horizontal(vertical) adjacent graph, the circuit block can move horizontally to its right(vertically upward) and the *available shifting distance* of each block can be obtained.

Refer to the LB-compacted floorplan in Fig. 2, the coordinate of the left-bottom point of the floorplan is generally defined as (0, 0) and the blocks in the floorplan are further labeled by the relative coordinates of X and Y directions as shown in Fig. 3(a). According to the labeled coordinates, the dimension of each block in this floorplan can be known and the horizontal and vertical adjacent graphs for the floorplan are shown in Fig. 3(b)(c), three horizontal longest paths, $B_4 \rightarrow B_{11} \rightarrow B_{15}$, $B_4 \rightarrow B_{11} \rightarrow B_{16} \rightarrow B_{17}$, and $B_5 \rightarrow B_{12} \rightarrow B_{16} \rightarrow B_{17}$, and two vertical longest paths, $B_{12} \rightarrow B_{11} \rightarrow B_{10} \rightarrow B_7 \rightarrow B_6$ and $B_{16} \rightarrow B_{15} \rightarrow B_{14} \rightarrow B_{13}$, can be obtained.
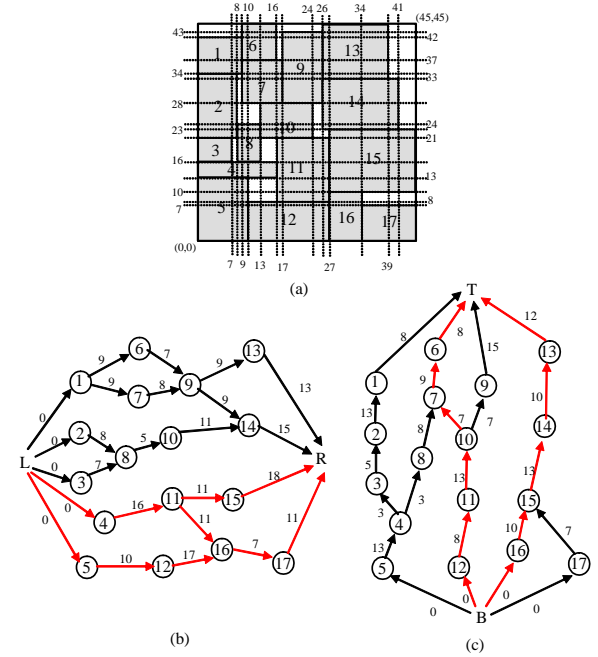

Fig. 3 An LB-compact floorplan and its adjacent graphs.

For any LB-compact floorplan, each block cannot move horizontally to its left and vertically downward without moving any block in the floorplan. To maintain all the neighborhood relations, all the horizontal(vertical) adjacent relations of any block, B_i, in the floorplan, F, can be bounded by the bottommost and topmost(leftmost and rightmost) adjacent relations, $RBPtr(B_i)$ and $RTPtr(B_i)$($TLPtr(B_i)$ and $TRPtr(B_i)$), of the block, B_i. Given an LB-compact floorplan, F, with the set of blocks, {B_1, B_2,…,B_n} and two dummy blocks, L and B, all the horizontal adjacent relations can be bound by using a horizontal bound list of $RBPtr(L)$, $RTPtr(L)$, $RBPtr(B_1)$, $RTPtr(B_1)$,…, $RBPtr(B_n)$ and $RTPtr(B_n)$, and all the vertical adjacent relations can be bound by using a vertical bound list of $TLPtr(B)$, $TRPtr(B)$, $TLPtr(B_1)$, $TRPtr(B_1)$,…, $TLPtr(B_n)$ and $TRPtr(B_n)$. Hence, all the adjacent relations in any LB-compact floorplan, F, can be bound by using the union of two bound lists named as a double bound list(DBL). Refer to the LB-compact floorplan in Fig. 2, its DBL representation can be illustrated in Fig. 4.
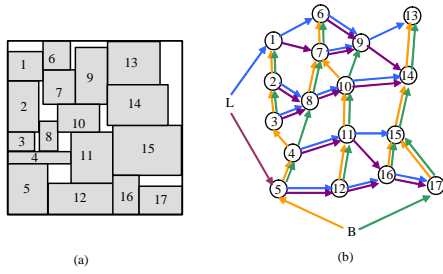
Fig. 4 DBL representation in an LB-compact floorplan

Beside the tight horizontal(vertical) adjacent relations in a DBL, there exist some loose horizontal(vertical) adjacent relations in an LB-compact floorplan. Given any pair of two blocks, B_i and B_j, in any LB-compact floorplan, F, if B_i is horizontally(vertically) visible to B_j, with limited empty space, a loose horizontal(vertical) adjacent relation, $B_i \to B_j$, between the blocks, B_i and B_j, will be defined. Refer to Fig. 2, five loose horizontal adjacent relations are defined as $B_5 \to B_{11}$, $B_8 \to B_{11}$, $B_2 \to B_7$, $B_2 \to B_{10}$ and $B_{10} \to B_{15}$, and six loose vertical adjacent relations are defined as $B_{12} \to B_4$, $B_4 \to B_2$, $B_4 \to B_{10}$, $B_8 \to B_1$, $B_{11} \to B_{14}$ and $B_{11} \to B_{14}$. According to the directed structure of the DBL representation and the loose adjacent relations in any LB-compact floorplan, all the blocks in the floorplan can be further unpacked and ordered into an LB(left-bottom) block list by running a topological sorting algorithm. As shown in Fig. 4(b), the LB block list can be unpacked and ordered as B_5, B_{12}, B_4, B_3, B_2, B_8, B_{11}, B_{10}, B_1, B_7, B_6, B_9, B_{16}, B_{17}, B_{15}, B_{14} and B_{13}.

IV. AREA-DRIVEN WHITE SPACE DISTRIBUTION BY USING PACKING AND GROUPING OPERATION

For any LB-compact floorplan, all the blocks are placed on the left-bottom corner in the floorplan plane, and there exists a floorplan contour from upper left to lower right to enclose all the blocks in the floorplan. From the positioning viewpoint of all the blocks in any LB-compact floorplan, the compact floorplan can be treated as the placement result of an ordered block list in the floorplan. As any block in the ordered block list is packed, the dynamic structure of a stair contour is maintained for the construction of the compact floorplan. Based on the dynamic structure of a stair contour, any block in the ordered block list can be packed into the original floorplan to create a new compact floorplan, and the left-bottom packing assignment for any block in an LB-compact floorplan can be called as *an LB-packing process*. Since the block assignment in any LB-compact floorplan is able to be done by using a LB-packing process, the compact floorplan can be called as an LB-packing-based floorplan.

Basically, area-driven space distribution can be completed based on the LB-packing-based process in any LB-compact floorplan and divided into two sequential phases: Unpacking and Packing. In the unpacking phase, all the space requirements can be estimated according to different design purposes in the original floorplan. The blocks in the original 2D floorplan can be unpacked and

ordered into an LB block list by using a topological sorting according to the tight and loose adjacent relations in the floorplan. As mentioned above, an LB-compact floorplan can be treated as the placement result of a sequence of given blocks in the floorplan by using an LB-packing process. To distribute all the required space into the original floorplan, the block and necessary required space must be grouped into a virtual block to be packed. In the packing phase, as any block in the ordered LB block list is packed into the processing floorplan, the block may be shifted by grouping with a horizontal or vertical space block with minimum increasing floorplan area. After distributing necessary the required space and packing the virtual block, the stair contour for the resultant floorplan must be modified. Until all the blocks in the LB block list are packed, a new floorplan will be obtained. Basically, the area-driven white space distribution will not be done until all the space requirements are satisfied. In Fig. 5, the design flow for area-driven white space distribution is shown.
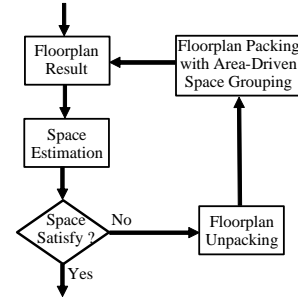

Fig. 5 Design flow for area-driven white space distribution

For the packing phase, the grouping issue of area-driven space is considered according to the available shifting distance of any block. To reduce the increasing floorplan area, the decision of the location of the required space becomes more important. As shown in Fig. 6, given a pair of adjacent blocks, B_j with its width, w_j, and its height, h_j, and B_i with its width, w_i, and its height, h_i, the grouping space can be obtained as $h_j(w_i - w_j)$. As the required space, $S_{i,j}$, is less than or equal to $h_j(w_i - w_j)$, the block, B_j, and the required space, $S_{i,j}$, can be grouped into a virtual block by inserting a horizontal space with its width, $S_{i,j}/h_j$, or a vertical space with its height, $S_{i,j}/w_j$. On the other hand, as the required space is larger than $h_j(w_i - w_j)$, the two adjacent blocks, B_j and B_i, and the required space, $S_{i,j}$, will be grouped into a virtual block by inserting the grouping space and a vertical space with its height, $(S_{i,j} - h_j(w_i - w_j))/w_i$.
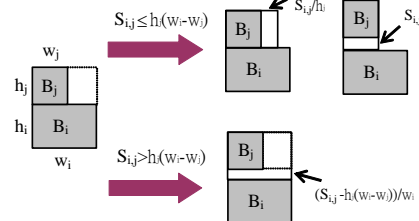
Fig. 6 Virtual block grouping with space requirement

Hence, the area-driven white space distribution can be used to satisfy all the space requirements for advanced design purposes from any LB-compact floorplan and the algorithm, *LBWSD*, is described as follows:

LBWSD(F, R)
Input: An LB-compact floorplan, F, with a set of blocks, {B₁, B₂,…, Bₙ},
  and a set of space requirements, R ;
  Initial left boundary L, and bottom boundary B;
  { Construct a DBL for the given floorplan, F;
    Find the loose horizontal and vertical adjacent relations for the
      given floorplan, F;
    Find an LB block list, BList, for the given floorplan, F, according to
      the directed structure of the DBL representation and the loose
      adjacent relations ; / BList = {Bₐ₍₁₎, Bₐ₍₂₎,…, Bₐ₍ₙ₎} /
    Contour = An initial contour, L -> B;
    Floorplan = An empty floorplan, F_LB;
    for (i==1; i<=n; i++)
      { Find the original stair contour for the block, Bₐ₍ᵢ₎;
        Assign the block, Bₐ₍ᵢ₎, onto the floorplan, F_LB;
        if (there is the space requirement between the block, Bₐ₍ᵢ₎, and
          any block involved in its stair contour)
          Create a virtual block and pack the virtual block onto the
            floorplan, F_LB, to satisfy the space requirement;
        Modify the stair contour of the floorplan, F_LB;
      }
    Output a final floorplan, F_LB, and Compute the floorplan area;
  }

Basically, the area-driven white space distribution can serve as a detailed floorplanning phase for advance design purposes. Refer to the LB-compact floorplan in Fig. 2, some blocks are shifted to satisfy all the space requirements in a floorplan plane as illustrated in Fig. 7.

Fig. 7 Area-driven white space distribution by block shifting

V. EXPERIMENTAL RESULTS

The LB-packing-based white space distribution, LBWSD, based on the grouping concept of the block and the necessary space in an LB-packing process has been implemented by using standard C++ language and run on a Pentium IV 2.8GHz machine. Four benchmark floorplans, xerox, hp, ami33 and ami49, are applied to redistribute the white space to minimize the final floorplan area with satisfying all the space requirements. Table I shows the original floorplan area, the dead space and all the space requirement of the tested benchmarks and the final

floorplan areas after running the proposed LBWSD algorithm. The experimental results show that the area increase is 1.4%~7.2% based on 4.2%~11.2% space requirement for the tested benchmarks in reasonable time. Clearly, the proposed LB-packing-based approach can redistribute the original white space to satisfy most of the space requirements.

TABLE I EXPERIMENTAL RESULTS FOR WHITE SPACE DISTRIBUTION

Circuits	Floorplan Area(mm²)	Dead Space(mm²)	Space Requirement(mm²)	LBST Area(mm²)	Time(s)
xerox	20.32	0.97	0.84(4.13%)	20.60(+1.38%)	0.01
hp	9.49	0.66	0.85(8.96%)	10.02(+5.58%)	0.01
ami33	1.25	0.09	0.14(11.20%)	1.34(+7.20%)	0.06
ami49	38.60	2.14	2.38(6.17%)	39.52(+2.38%)	0.11

VI. CONCLUSIONS

Based on the LB-packing-based property in an LB-compact floorplan, some white space for advanced design requirement is considered. By using the grouping concept of the block and the necessary space, the white space in a floorplan is redistributed to minimize the final floorplan area with satisfying all the space requirements. Basically, the area-driven white space distribution can serve as a detailed floorplanning phase for advance design purposes.

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