行政院國家科學委員會專題研究計畫 成果報告

應用於下世代 CMOS 元件之簡易且新穎式雷射製程技術
研究成果報告(精簡版)

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處 理 方 式 ：本計畫涉及專利或其他智慧財產權，2 年後可公開查詢

中 華 民 國 99 年 09 月 30 日

行政院國家科學委員會補助專題研究計畫 ■成果報告 □期中進度報告

應用於下世代 CMOS 元件之簡易且新穎式雷射製程技術

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計畫主持人：吳建宏
共同主持人：
計畫參與人員：吳建宏、洪瑞陽、黃俊哲、林智偉

成果報告類型(依經費核定清單規定繳交)：■精簡報告　□完整報告

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中　華　民　國　99 年 09 月 29 日

行政院國家科學委員會研究計畫成果報告

應用於下世代 CMOS 元件之簡易且新穎式雷射製程技術

計畫編號：NSC 98－2218－E－216－002－

全程執行期間：98 年 04 月 01 日至 99 年 06 月 31 日

主持人：吳建宏 助理教授 執行單位：中華大學微電子工程系

中文摘要

對於發展下世代 CMOS 元件之簡易且新穎式雷射技術而言，將是半導界的主流。本研究團隊於研發出金屬閘極搭配氧化鑭高介電係數介電層的 n 型金氧半場效電晶體。接著我們更進一步利用高介電常數氧化鑭來製作鍺金氧半場效電晶體，二氧化矽做為介面層，氮化鉭做為金屬閘極。利用雷射退火的方式去達到改善元件的特性，得到低的片電阻值 68 Ω/sq，理想因子為 1.3 和在源極和汲極的 PN 接面得到了大的順向/逆向電流.雷射退火後的閘極優先 TaN/La2O3/SiO2/Ge n 型金氧半場效電晶體，在等效氧化層厚度為 1.9nm 下，顯示出高的遷移率 603 cm^2/Vs，在 0.75 MV/cm 下遷移率為 304 cm^2/Vs。

一、 簡介

The small bandgap (E_G) Ge shows high potential for MOSFET application due to both higher electron and hole mobility than Si. However, the difficult challenges are the high leakage current of small E_G Ge, poor high-κ/Ge interface property, and low doping activation at ion-implanted source-drain [1]-[16]. To address the leakage current issue, we pioneered the defect-free Ge-on-insulator (GOI or GeOI)[1] structure and ultra-thin body Ge-on-Si[11]. The high-κ/Ge interface property can also be improved by using an ultra-thin robust SiO_2 interfacial layer. Nevertheless, the poor doping activation by RTA is still an issue, while the high temperature RTA degrades the mobility by Ge out-diffusion and forming poor interface. Although a gate-last process with GeO_2 dielectric was developed for this purpose [11]-[15], the *gate-first* process is still attractive for much simple process. Besides, the filling in narrower gate opening with both high-κ and metal using gate-last process is another concern, since Ge is expected to implement in 15~10 nm node CMOS. In this paper we have used low energy laser annealing [16] to improve the doping activation of ion-implanted source-drain and preserve good high-κ/Ge interface, while laser annealing is also essential for ultra-shallow junction. High performance *gate-first* $TaN/La_2O_3/SiO_2/Ge$ n-MOSFET was obtained using laser annealing, with high peak mobility of 603 cm^2/Vs and 0.75 MV/cm mobility of 304 cm^2/Vs at small 1.9 nm EOT. The good mobility at high effective electric field (E_{eff}) is required for highly scaled MOSFET with small EOT. These results are beyond the best reported data for *gate-first* metal-gate/high-κ/Ge n-MOSFET at small

EOT <2 nm.

二、 實驗步驟

Standard 2-in p-type Ge (100) wafers were used for the experiments. After standard clean, ultra-thin 0.8 nm SiO2 and 2 nm La2O3 were deposited by physical vapor deposition (PVD) and followed by post-deposition anneal under oxygen ambient. After 150 nm TaN gate metal deposition and patterning, the n+ source-drain regions are formed by As+ implantation at 25 KeV and 5×1015 cm-2 dose. Then scanned KrF laser annealing (248 nm, <30 ns pulse) was applied to activate the implanted dopant [6],[16]-[19]. The junction characteristics and sheet resistance were measured to characterize the effect of laser annealing. Finally, Al metal contacts were added to source-drain and form the Ge n-MOSFET. The fabricated devices were characterized by C-V and I-V measurements using an HP4284A precision LCR meter and HP4156C semiconductor parameter analyzer, respectively.

三、 結果與討論

Figures 1(a) and 1(b) show the sheet resistance (Rs) and n+/p junction characteristics of As+-implanted Ge after laser annealing. The increasing laser energy density improves Rs, the junction ideality factor (n) and forward current, while still maintaining a low reserve leakage current. The Rs decreases rapidly with increasing laser fluence (energy/area) to 0.16 J/cm2. This value is significantly lower than previous 0.36 J/cm2 value for Si device anneal [16] that is due to the much lower melting temperature of Ge than Si. The lower laser fluence is important to decrease the energy absorbed by TaN gate that can cause unwanted interface reaction and Vfb roll-off [16]. The Rs as low as 68 /sq was obtained at 0.2 J/cm2 laser fluence that is 40% better than the 112 /sq Rs using RTA at 550oC. Small n-factor of 1.3 and very large ~105 forward/reverse current ratio are measured for n+/p junction using laser annealing and also better than the control RTA devices. The higher forward current in the n+/p junction is crucial to reach the higher drive current of Ge n-MOSFET.

Figures 2(a) and 2(b) show the C-V and J-V characteristics of TaN/La2O3/SiO2/Ge devices, where slight Vfb shift and increasing gate current were found by laser annealing. An EOT of 1.9 nm was obtained from quantum-mechanical C-V calculation with Ge material values [14],[16]. The effect of laser annealing on gate dielectric was further examined by cross-sectional TEM. Still sharp interfacial SiO2 layer was observed by laser annealing that gives the good C-V characteristics. This is due to the low 0.2 J/cm2 laser fluence, although it is high enough to melt and crystallize the ion-implanted Ge. Besides, 1/3 energy was reflected at top TaN surface from the measured reflectivity [16]. These further lower the energy absorbed by high- /Ge interface. The higher gate leakage current may be related to TaN/La2O3 inter-diffusion by laser annealing, although more detailed study is needed.

Figures 3(a) and 3(b) show the Id-Vd and Id-Vg characteristics of La2O3/SiO2/Ge n-MOSFETs using laser annealing. Well behaved transistor characteristics were reached, with a good sub-threshold swing of 125 mV/dec. A negative threshold voltage (Vt) of -0.47 V is due to the negative Vfb measured from C-V characteristics in Fig. 2(a). Although this indicates less Fermi-level pinning, further adjusting the Vt to positive value is needed. Figure 4 further shows the mobility over a wide Eeff range. High peak

mobility of 603 cm2/Vs and 0.75 MV/cm mobility of 304 cm2/Vs are reached for the Ge n-MOSFETs using laser anneal, which is the highest electron mobility for gate-first Ge n-MOSFET.

四、 結論

Using low energy laser anneal on $TaN/La_2O_3/SiO_2$ Ge n-MOSFETs, small junction *n*-factor of 1.3, big 10^5 n^+/p junction forward/reverse current, high 603 cm^2/Vs peak mobility and good high-field (0.75 MV/cm) mobility of 304 cm^2/Vs were reached simultaneously at small EOT of 1.9 nm.

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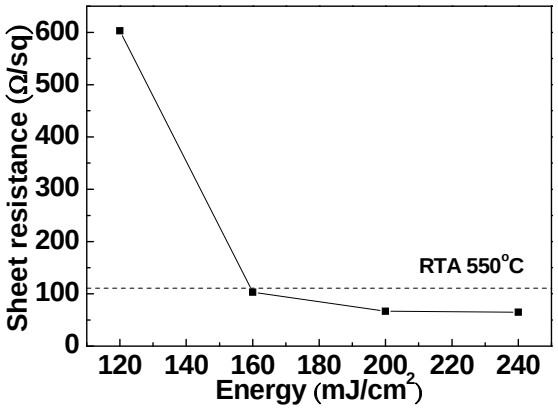
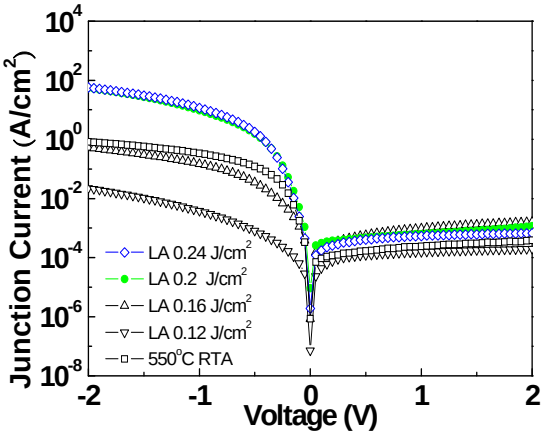
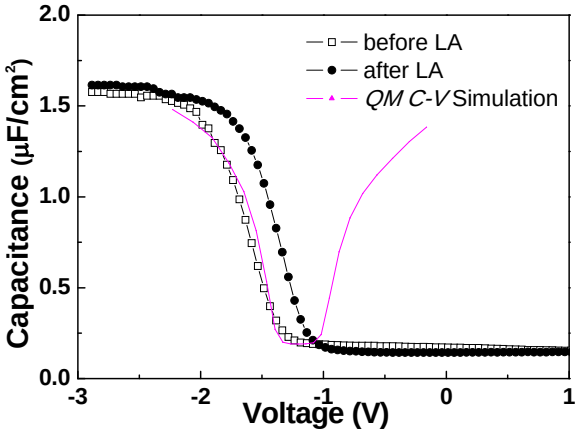


(a)



(b)

Fig. 1. (a) Sheet resistance and (b) n+/p junction characteristics of As+-implanted Ge after laser annealing.



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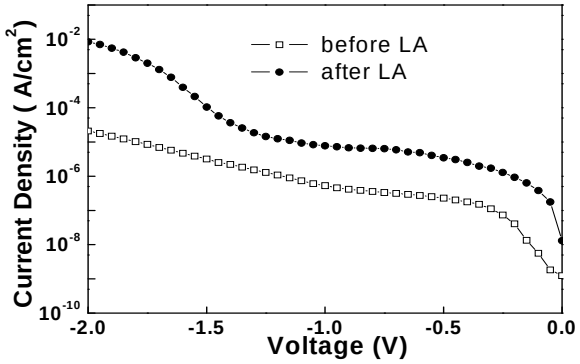
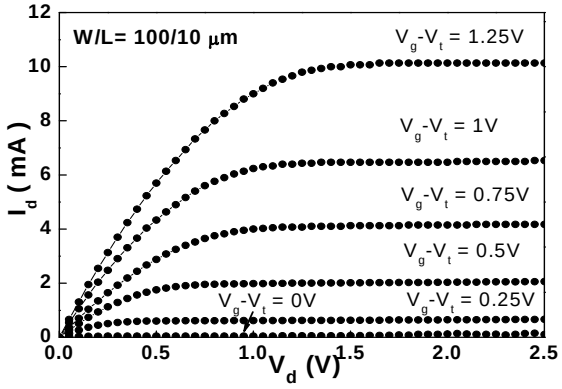


(b)

Fig. 2. (a) *C-V* and (b) *J-V* characteristics of TaN/La_2O_3/SiO_2/Ge n-MOS capacitors before and laser annealing.



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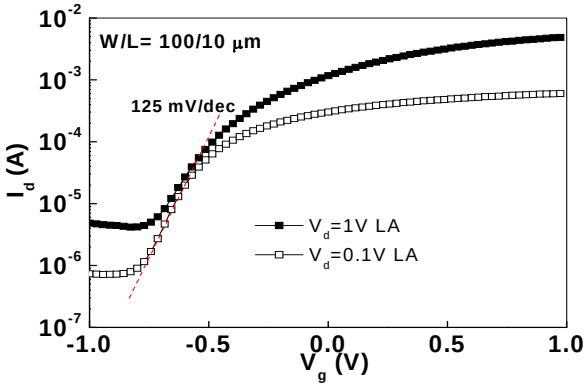

(b)

Fig. 3. (a) Id-Vd and (b) Id-Vg of gate-first TaN/La2O3/SiO2/Ge n-MOSFET using laser annealing.

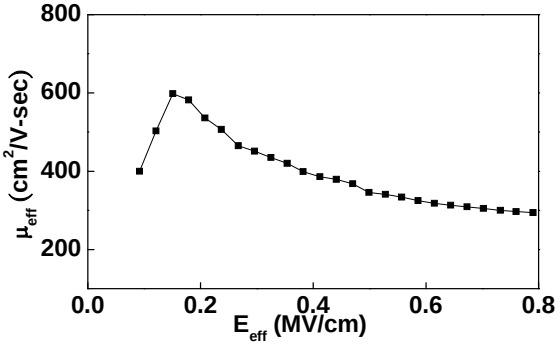

Fig. 4. The electron mobility as a function of effective electric field of $TaN/La_2O_3/SiO_2/Ge$ *n*-MOSFETs using laser annealing.

行政院國家科學委員會補助團隊參與國際學術組織會議報告

98 年 7 月 13 日

報告人姓名	吳建宏	服務機構	中華大學 微電子系	職稱	助理教授
會議正式名稱	中文：2009 年 IEEE 北東討論室在電路與系統之 TAISA 研討會				
	英文：2009 IEEE North-East Workshop on Circuits and Systems and TAISA Conference				
會 議 時 間	自 98 年 6 月 28 日至 98 年 7 月 1 日		地點（國、州、城市）	法國 土魯斯	

報告內容應包括下列各項：

一、參加會議經過

本次會議共 4 天，所探討的主題，除了工業界十分重視的 Computer and System architecture, RF, digital, analog and mixed-signal circuit design, Data and signal processing, Microsystems, memories, sensors and associated analog processing Mathematical methods and design tools Telecommunications, radio-frequencies and microwaves 等，而歐洲也是全球太陽能電池發展最先進的地方順道了解一下城市的綠能。此大會之 plenary talks 邀請國際知名學者演講。本會議之水準相當不錯。

二、與會心得

在我所參加的 RF circuit 方面，目前於國際半導體藍圖規化中，將於未來 32nm node 之技術中。然而目前技術上尚有許多的困難及挑戰，如何達到最好的效能，如何降低漏電流，操作更高的頻段。然而在歐洲研發中心-IMEC 的推動下，相信未來將有長足的進步。

在會場還遇到大陸方面的學者，相當有興趣來台灣做研究或是就業，也有邀請她來學校當訪問學者。有關 RF 電路的技術，目前最新的消息爲國外大廠紛紛準備上生產線，故國內 IC 公司亦預計明後年能上線，以利國際間的競爭。

我亦在大會中提及，台灣乃是全球代工與電路研發中心，故生產成本將不斷下降，因此未必歐洲可領先。此觀點亦獲得大家的認可。

三、考察參觀活動（無是項活動者省略）

無

四、建議事項

此次參加本會議，驚覺中國大陸所參與的人數遠超過台灣，而其所發表的論文品質，亦具國際化的水準。國內應多鼓勵同仁參加，以確保領先的地位。

五、其他

NEWCASTAISA 會議論文一份

A Wideband 0.18 μm CMOS LNA with RC-Feedback Topology for UWB Applications

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Abstract **- A 0.18 μm CMOS low noise amplifier using RC-feedback topology is proposed with optimized matching, gain, noise, linearity and area for UWB applications. The IC prototype achieved 9.5 dB of average power gain, low 3.4 dB noise figure (NF), -9.2 dB input match, -13.5 dB return loss, -6 dBm of IIP3 and only 0.54 mm^2 size with 15 mW power consumption. Good agreement between the simulated and measured results is found.**

I. Introduction

The Federal Communications Commission (FCC) has distributed 7500 MHz bandwidth for ultra-wideband (UWB) applications. Ultra-wideband technology using the unlicensed frequency band from 3.1 to 10.6 GHz has become much interest of broadband wireless communication due to its high data rates, low power transmission, robustness for multi-path fading and low power dissipation. Among possible applications, UWB technology may be used for imaging systems, vehicular and ground penetrating radars, and communication systems. For such broadband applications, the low noise amplifier (LNA) is the first stage in the UWB receiver. It must provide good input impedance matching, low power consumption, low noise performance and sufficient gain with good S/N for the following stages, and small size over the entire frequency band [1]-[13]. Recently, the CMOS technology is a candidate for UWB LNA system [7]-[19] when considering the time to market, hardware cost, the degree of difficulty, and high integration with baseband digital circuits – for a good System-on-Chip (SoC) solution. However, these performance requirements for UWB are very challenging using CMOS technology. This is because the CMOS technology can only provide small gain at high frequency, low cut-off frequency (f_T) [20]-[22], significant substrate loss [23]-[24] and poor inductor Q-factors [22] compared with GaAs technology. Several different circuit approaches, including distributed amplifier (DA), LC ladder, current-reused, shunt feedback, etc., have been proposed to overcome these issues [7]-[19].

The RC-feedback cascode topology is one of the main methods for wideband amplifier design [11]-[16]. The RC-feedback cascode configuration can provide good input matching and improve gain flatness. However, the challenge of this technique is very wide bandwidth along with low noise and high gain. In this work an ultra-wideband CMOS LNA is proposed a cascode amplifier with three stages: new RC-feedback cascode topology, LC shunt configuration and output current buffer technology, implemented in 0.18 μm CMOS technology. With new RC-feedback cascade connection and LC shunt techniques, this LNA achieved a 9.5 dB average power gain, a 3.4 dB NF, input reflect loss less than -9.2 dB, output return loss less than -13.5 dB and the input IIP3 is -6 dBm from ultra-wide band LNA circuit. These results are suitable for UWB LNA circuit application.

II. Circuit Design

The UWB LNA requires high gain, low noise figure and high linearity over the entire band with low power consumption. The LNA also needs to have a good input mating over the whole band to capture the transmitted RF energy efficiently. Figure 1 shows a schematic of the proposed three stages amplifier. The first stage is the capacitance-resistance feedback cascode topology that provides high gain, wider bandwidth, better stability and well reverse isolation. The middle stage is an inductor-capacitor parallel configuration (L_B//C_B) to pull up high frequency gain. The output stage is a simple current buffer that gives broadband output impedance of 50 Ω for measurement purposes. This circuit was designed with Agilent's Design System (ADS), and implemented in TSMC's 0.18 μm RF CMOS technology.

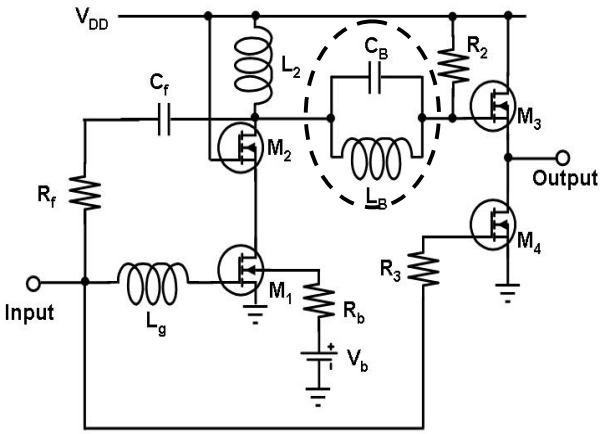

Fig. 1. Schematic of the ADS-designed UWB CMOS RC-feedback LNA circuit. The dashed circle is L_B//C_B shunt topology.

For input matching, we used RC-feedback cascode topology for matching. The cascode configuration can reduce the high frequency roll-off of the input devices due to the Miller effect. It provides input and output matching independently. We can select Z_f (R_f and C_f components) to achieve good input matching and high gain. The output stage of the RC-feedback LNA circuit is used current buffer (M_3 and M_4 transistors) to tune the whole frequency to achieve 50 Ω. The M_3 is the source follower and the M_4 provide the stable current source for M_3. We only fine tune the bias and transistors size to achieve good output matching.

Among several topologies that provide a gain over a wideband, the RC-feedback loop is one of the most popular to use in amplifiers circuit for its wideband input matching and good linearity [11]-[13]. The substrate bias of transistor M_1 is used to raise the gain and reduce the power dissipation. However, the gain was confined at high frequency due to gate-drain capacitance and gate-source capacitance. For further rise up the gain at higher frequency, an inductor-capacitor parallel configuration (L_B//C_B) was connected to the second stages to extend bandwidth as the dashed circle in Fig. 1. The L_B//C_B is chosen to resonate at 10.6GHz for the bandwidth extension. The power gain (S_{21}) can increase at high frequency. The wide band and high gain was obtained in our LNA circuit design.

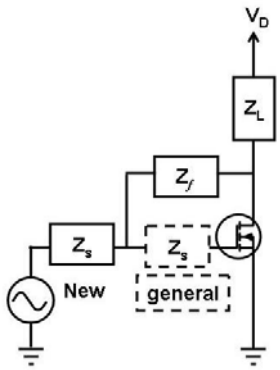

Fig. 2. The schematic of input stage for RC-feedback UWB LNA added noise circuit. The solid line is our work and the dash line is general design for comparison.

The RC-feedback topology in first stage is dominated the noise characteristics for LNA. To analysis the noise performance of the RC-feedback CMOS amplifier, the noise sources are added to the schematic circuit of first stage as shown in Fig. 2, also comparison with general circuit design [12]-[17]. Compare with general circuits, the proposed feedback topology is connected in front of the matching gate inductor (L_g). From the noise circuit, the total noise v_i^2 of the general design circuit is one item ($i_f^2 R_{Lg}^2$) more than that of our circuit due to the noise current i_f does not go through the L_g. The NF_{min} of new FB circuit and general design are compared using ADS simulated as shown in Fig. 3. The NF can be reduced 0.54 dB at high frequency. Therefore, the noise figure can be reduced using new feedback topology circuit. A high voltage and low noise UWB LNA can be achieved. The observation of our design is presented in the following section.

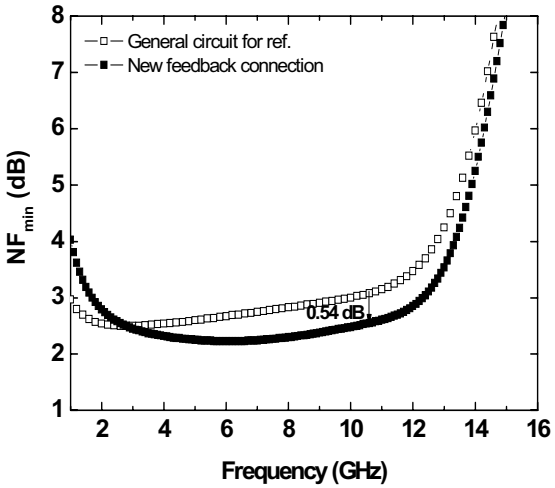

Fig. 3. Simulated noise figure (NF_{min}) using new feedback topology and general circuit for comparison.

III. Results And Discussion

The CMOS UWB LNA was tested via on-wafer probing. A network analyzer and ATN-NP5B noise-parameter system meter were used to measure the small-signal *S*-parameters and *NF* over the frequency range from 1 to 16 GHz. Fabricated in 0.18 μm 1P6M standard CMOS process this prototype chip using power supply of 1.8 V consumes 15 mW including the output buffer stage. The microphotograph of fabricated CMOS UWB LNA with a chip size 0.54 mm^2 including the probe pads is shown in Figure 3.

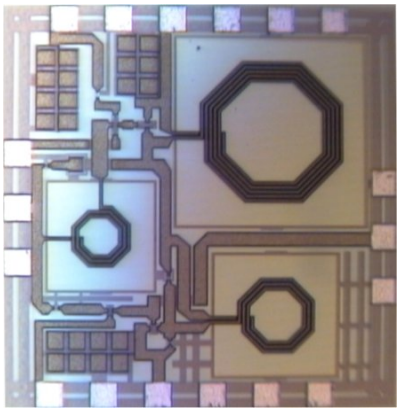

Fig. 3. Image of the fabricated RC-Feedback UWB LNA.

Figures 4 and 5 show the two-port measured S-parameters from 1 GHz to 16 GHz. Figure 4 shows the dependence of measured input reflection coefficient (S_{11}) and output return loss (S_{22}) on frequency. The measured S_{11} was lower than -9.2 dB for input matching across the frequency band of 3.1~10.6 GHz. The measured S_{22} was less than -13.5 dB for output matching over a 3.1~10.6 GHz range. In Figure 5 the measured forward gains (S_{21}) and reverse isolation (S_{12}) are reported for

the UWB LNA circuit. The S_{21} displays a maximum gain of 11.7 dB at 3.1 GHz and the average S_{21} value over the 3.1-10.6 GHz frequency band is 9.5 dB. With RC-feedback cascade topology, the bandwidth extends to cover from 3.1 to 10.6 GHz. An excellent S_{12} of less than -25.7 dB was obtained due to effective cascode configuration. It is noted that the input impedance was optimized for low noise figure while keeping the corresponding return loss at an acceptable level.

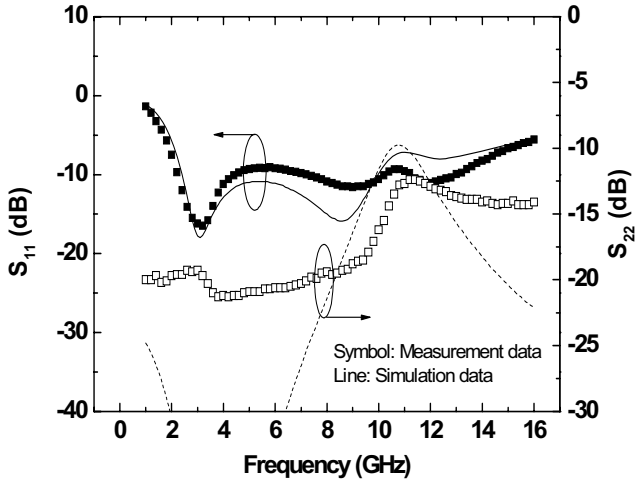

Fig. 4. Measured and simulated input return loss (S_{11}) and output loss (S_{22}) of the RC-Feedback UWB LNA.

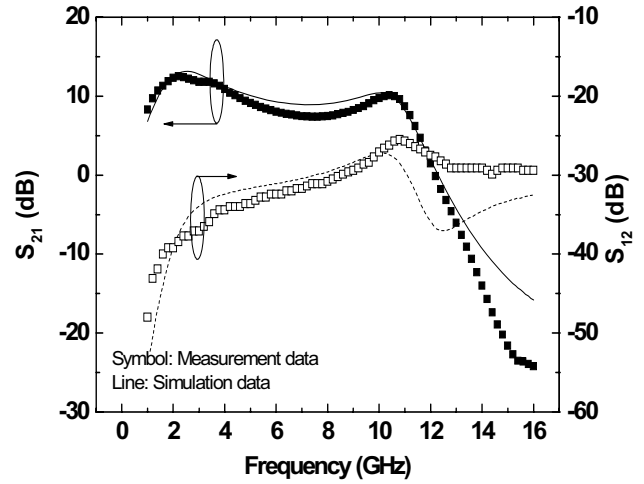

Fig. 5. Measured and simulated power gain (S_{21}) and reverse isolation (S_{12}) of the RC-Feedback UWB LNA.

To optimize the performance, the transistors have been sized to provide good noise characteristics, while allowing a good input impedance matching over the required bandwidth. The measured NF of the implemented amplifier is shown in Figure 6. The measured NF shows a minimum value of 3.41 dB at 9 GHz. The measured NF range was 3.41~ 4.04 dB over the 3.1~10.6 GHz range. Figure 7 shows the two-tone test for third-order intermodulation distortion of the UWB CMOS LNA circuit. The third order input intercept point (IIP3) is -6 dBm.

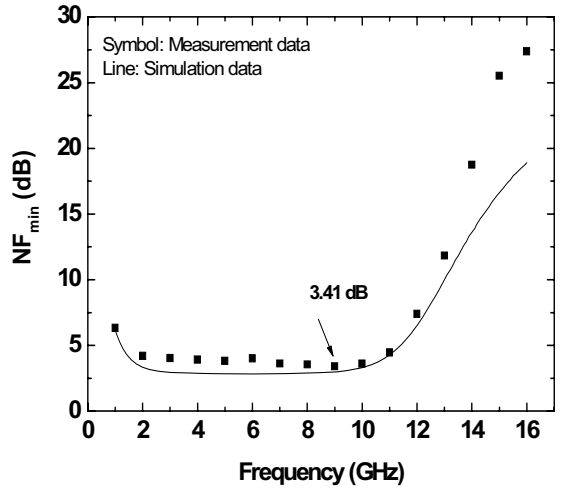

Fig. 6. Measured and simulated noise figure (NF_{min}) of the RC-Feedback UWB LNA.

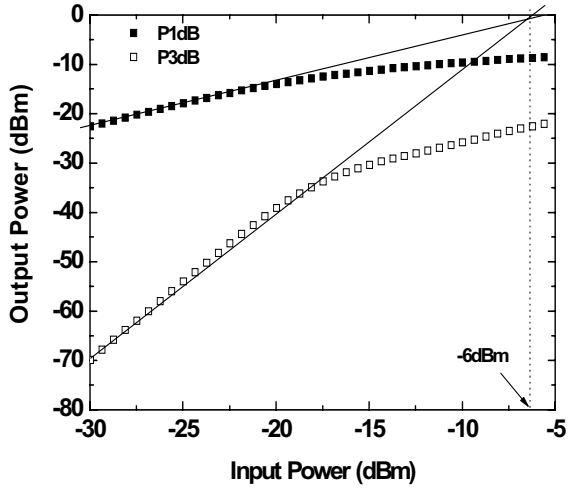

Fig. 7. Measured IIP3 of the RC-Feedback UWB LNA.

Table 1 summarizes the measured performance of the LNA and compares the other reported circuit performance. Our proposed CMOS LNA can achieve a wide bandwidth, high gain, good linearity, low *NF* and low power consumption, and compares well with other published reports [15]-[17].

Table 1. Comparison of LNA circuit performance: published and this work.

Ref.	**[15]**	**[16]**	**[17]**	**This Work**
BW (GHz)	2.8 ~ 7.2	3.1 ~ 10.6	1.2 ~ 11.9	3.1 ~ 10.6
***S*$_{11}$ (dB)**	< -4	<-9.7	< -11	< -9.2
***S*$_{22}$ (dB)**	< -7.5	N/A	N/A	< -13.5
Gain (dB)	16 ~ 19.5	7.4 ~ 9.2	5 ~ 9.7	7.5 ~ 11.7
***NF*$_{min}$ (dB)**	3.1 ~3.8	4.1 ~ 7	4.2 ~ 5.1	3.4 ~4.04
IIP3 (dBm)	-1	7.25	-6.2	-6
PD (mW)	32	23.5	20	15
Area (mm^2)	1.63	0.78	0.59	0.54
Topology	0.18 µm Feedback	0.18 µm Feedback	0.18 µm Noise-Canceling	0.18 µm Feedback

IV Conclusion

A CMOS UWB LNA with new RC-feedback connection has been designed. This UWB LNA exhibited a high 11.7 dB gain, low 3.4 dB NF, input reflect loss less than -9.2 dB, output return loss less than -13.5 dB and the input IIP3 is -6 dBm from 3.1 to 10.6 GHz, while only 15 mW power dissipation. The fabricated LNA satisfies UWB LNA system requirements.

ACKNOWLEDGEMENT

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無研發成果推廣資料

98 年度專題研究計畫研究成果彙整表

計畫主持人：吳建宏	計畫編號：98-2218-E-216-002-
計畫名稱：應用於下世代 CMOS 元件之簡易且新穎式雷射製程技術	

成果項目	量化			單位	備註（質化說明：如數個計畫共同成果、成果列為該期刊之封面故事...等）
	實際已達成數（被接受或已發表）	預期總達成數(含實際已達成數)	本計畫實際貢獻百分比		

國內	論文著作	期刊論文	2	2	100%	篇	1.Nai-Chao Su, Shui-Jinn Wang, Chin-Chuan Huang, Yu-Han Chen, Hao-Yuan Huang, Chen-Kuo Chiang, Chien-Hung Wu, and Albert Chin, ’ The Role of High-κ TiHfO Gate Dielectric in Sputtered ZnO Thin-Film Transistors, ’ Jpn. J. Appl. Phys., 49 (2010) 04DA12 （SCI=1.138） 2.C. H. Wu, C. K. Chiang, Y. H. Chen,N. C. Su, S. J. Wang, C. C. Huang, K. L. Kao, M. S. Yeh and I. J. Hsieh, ’ Defect Density Extraction of high-κ Dielectric Gate Stack by Combining Charge Pumping and Low Frequency Measurement,’ Chung Hua Journal of Science and Engineering, Vol. 7, No. 3, pp.79-83, 2009.
		研究報告/技術報告	0	0	100%		
		研討會論文	0	0	100%		
		專書	0	0	100%		
	專利	申請中件數	0	0	100%	件	
		已獲得件數	0	0	100%		

	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（本國籍）	碩士生	0	0	100%	人次	
		博士生	0	0	100%		
		博士後研究員	0	0	100%		
		專任助理	0	0	0%		無
國外	論文著作	期刊論文	0	0	100%	篇	
		研究報告/技術報告	0	0	100%		
		研討會論文	0	0	100%		
		專書	0	0	100%	章/本	
	專利	申請中件數	0	0	100%	件	
		已獲得件數	0	0	100%		
	技術移轉	件數	0	0	100%	件	
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	參與計畫人力（外國籍）	碩士生	0	0	100%	人次	
		博士生	0	0	100%		
		博士後研究員	0	0	100%		
		專任助理	0	0	100%		
其他成果 (無法以量化表達之成果如辦理學術活動、獲得獎項、重要國際合作、研究成果國際影響力及其他協助產業技術發展之具體效益事項等，請以文字敘述填列。)							

	成果項目	量化	名稱或內容性質簡述
科教處計畫加填項目	測驗工具(含質性與量性)	0	
	課程/模組	0	
	電腦及網路系統或工具	0	
	教材	0	
	舉辦之活動/競賽	0	
	研討會/工作坊	0	
	電子報、網站	0	
	計畫成果推廣之參與（閱聽）人數		

國科會補助專題研究計畫成果報告自評表

請就研究內容與原計畫相符程度、達成預期目標情況、研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）、是否適合在學術期刊發表或申請專利、主要發現或其他有關價值等，作一綜合評估。

1. 請就研究內容與原計畫相符程度、達成預期目標情況作一綜合評估

■達成目標

□未達成目標（請說明，以 100 字為限）

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□因故實驗中斷

□其他原因

說明：

2. 研究成果在學術期刊發表或申請專利等情形：

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技轉：□已技轉 □洽談中 ■無

其他：(以 100 字為限)

3. 請依學術成就、技術創新、社會影響等方面，評估研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）(以 500 字為限)

對於發展下世代 CMOS 元件之簡易且新穎式雷射技術而言，將是半導界的主流。本研究團隊於研發出金屬閘極搭配氧化鑭高介電係數介電層的 n 型金氧半場效電晶體。接著我們更進一步利用高介電常數氧化鑭來製作鍺金氧半場效電晶體，二氧化矽做為介面層，氮化鉭做為金屬閘極。利用雷射退火的方式去達到改善元件的特性，得到相當優異的元件特性，相信未來業界也一定會陸續採用這樣的技術和製程。這樣的計畫也陸續發表了數篇論文和研討會論文。