PARAMETER STUDY TO THE INTERPOSER STRESS ANALYSIS OF FINE PITCH 3-D STACK PACKAGE

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Abstract

Through-Silicon Vias (TSVs) have recently aroused much interest because it is a key enabling technology for three-dimensional (3-D) integrated circuit stacking and silicon interposer technology. In this study, a 3-D 1/8th symmetrical nonlinear finite element model of a stack die TSV package was developed using ANSYS finite element simulation code. The model was used to optimize the package for robust design and to determine design rules to enhance TSV reliability in view of TSV stress. An L9 Taguchi matrix was developed to investigate the effects of dielectric thickness, TSV diameter, and interposer thickness on TSV stresses that could possibly occur during a temperature cycling test in the range of 0 °C to 100 °C. The TSV stress index was based on the end of high-dwell temperature in the third cycle due to a 75 °C temperature difference compared with room temperature of 25 °C. Three levels were chosen for each parameter to cover the ranges of interest. The results show that the best combination is 1 m of insulation thickness, 50 m of TSV diameter, and 400 m of interposer thickness. The sensitivity degree order of system noise is interposer thickness, TSV diameter, and dielectric thickness. These could be used as guides for further similar 3-D stack packages design.

Keyword：3-D STACK PACKAGE; TAGUCHI METHOD;TSV