

Iridium Nanocrystal Thin-Film Transistor Nonvolatile Memory with  
Si<sub>3</sub>N<sub>4</sub>/SiO<sub>2</sub> Stack of Asymmetric Tunnel Barrier

吳建宏, 王泰瑞, 呂天麟, 劉育成, Shih-Wei Hung, 謝英家, Cheng-Tzu Kuo

Electrical Engineering  
Engineering

Abstract

Iridium nanocrystals (Ir-NCs) lying on the Si<sub>3</sub>N<sub>4</sub>/SiO<sub>2</sub> tunneling layer have been demonstrated and Ir-NC-assisted thin-film transistor nonvolatile memory devices were successfully developed. Results show that Ir-NCs with a number density of  $6 \times 10^{11} \text{ cm}^{-2}$  and a particle diameter of 4 to 12 nm can successfully be fabricated as charge trapping centers. Owing to the asymmetric SiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub> tunneling layer that increases programming/erasing efficiency, a significant memory window of 5.5 V has potential to be applied to multibit memory devices. Furthermore, after 104 s, the memory window is still about 4.0 V in logic states.

Keyword : Iridium nanocrystals and nonvolatile memory devices