Finite Element Analysis of 90-nm Cu/Low-K Interconnection Interactions with Chip-Packaging Factors

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Abstract

The multiple zoom-in modeling technique is used to investigate the stress cracking and voiding at the via and low-K delamination between a Cu metal trace and low-K dielectric. The die thickness, substrate body size, BT core thickness, through hole density and bumping pattern are five chip-packaging factors for these parametric studies. The global HFCBGA package model was validated first using the moiré interferometery method. After that, the whole package was subjected to a temperature load of 125℃ to -55℃ to evaluate the Cu/low-K interconnection reliability. During the simulation process, the determined results at each modeling level were used to correlate the observed failure mechanisms. The FEM predictions agreed with the existing failure modes. Through parametric studies, the substrate body size and bumping pattern were identified as major chip-packaging factors that especially influenced low-K delamination. A larger body size and uniform bump pattern can reduce the low-K delamination risk level. The remaining factors are minor with less than a 2% normality variation.

Keyword：Cu/low-K interconnection, HFCBGA package, low-K delamination