Design of Direct Digital Frequency Synthesizers Based on Unilateral Second-Order Approximations

林國珍, 張哲銘

Electronics Engineering

Engineering

kuojenlin@chu.edu.tw

Abstract

A new sine amplitude compression technique employing unilateral second-order approximation methods is proposed for a direct digital frequency synthesizer. The technique uses a second-order polynomial approximation above or below the ideal sine function to reduce the errors. Both the approximation methods can save 10 bits per word in a ROM. By using Horner's rule and some design skills, we can reduce more arithmetic operations. A Xilinx FPGA design demonstrates the spurious free dynamic range of the proposed architecture.

Keyword：DDFS, amplitude compression technique, second-order polynomial approximation, Horner's rule