Multiplierless, Folded Reconfigurable Architecture for VLSI Wavelet Filter

宋志雲,辛錫進
Microelectronics Engineering
Engineering
bobsung@btcx.com.tw

Abstract

In this paper, the high-efficient and reconfigurable architectures for the 9/7-5/3 discrete wavelet transform (DWT) based on convolution scheme are proposed. The proposed parallel and pipelined architectures consist of a high-pass filter (HF) and a low-pass filter (LF). The critical paths of the proposed architectures are reduced. Filter coefficients of the biorthogonal 9/7-5/3 wavelet low-pass filter are quantized before implementation in the high-speed computation hardware. In the proposed architectures, all multiplications are performed using less shifts and additions. The proposed reconfigurable architecture is 100% hardware utilization and ultra low-power. The proposed reconfigurable architectures have regular structure, simple control flow, high throughput and high scalability. Thus, they are very suitable for new-generation image compression systems, such as JPEG-2000.

Keyword：Folded reconfigurable architecture, 9/7-5/3 discrete wavelet transform (DWT), high-pass filter (HF), low-pass filter (LF), convolution scheme.