FPGA Implementation of High Performance DCT/IDCT Processor

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Abstract

Discrete cosine transform (DCT) and inverse DCT (IDCT) are important in various image processing systems. In this paper, a novel linear array of simple compuations is pro[osed for DCT/IDCT, which is based on the subband decompositions of a signal. To increase throughput as well as decrease hardware cost, the input and output signals data are deliberately reordered. The proposed 8-point DCT/IDCT processor with three multipliers, simple adders, and less registers and ROM storing the immediate results and cofficients, respectively, has been implemented using FPGA. The linear-array archtecture with computation complexity O(3N/8) for DCT/IDCT is fully pipelined and high scable. The proposed aschitectures for 2-D DCT/IDCT processors not onlysimplify hardware but also reduce the power comsumption.

Keyword：DCT/IDCT, subband decomposition, linear array, pipelined, scable. FPGA