A Novel VLSI Architecture for Digital Frequency Synthesizer

宋志雲,柯律廷,陳竹一,辛錫進,謝曜式
Electronics Engineering
Engineering
bobsung@chu.edu.tw

Abstract

This paper presents a novel algorithm and architecture for digital frequency synthesis (DFS). It is based on a simple difference equation. Simulation results show that the proposed DFS algorithm is preferable to the conventional phase-locked-loop frequency synthesizer and the direct digital frequency synthesizer in terms of the spurious-free dynamic range (SFDR) and the peak-signal-to-noise ratio (PSNR). Specifically, the results of SFDR and PSNR are more than 186.91 dBc and 127.74 dB, respectively. Moreover, an efficient DFS architecture for VLSI implementation is also proposed, which has the advantage of saving hardware cost and power consumption.

Keyword：Digital frequency synthesis, Difference equation, SFDR, PSNR, VLSI.