Embedded 3-D Integrated Inductor for Voltage-Controlled SAW Oscillator

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Abstract

cso has a crucial application in timing synchronization, such as clock recovery due to its high
frequency stability. Low jitter performance is important for high quality service. In this study an
integrated VCSO with Pierce configuration was developed as shown in Fig. 1. Except for the SAW resonator,
a phase shift with π-type LC circuit was embedded to achieve the Barkhausen's oscillation condition. A 3-D
inductor as shown in Fig. 2 was constructed by the standard CMOS process to save the chip area. Its rf
behavior was first calculated by the EM simulator. The related lumped model as shown in Fig. 3 was then
extracted. For a 14 nH inductance, the area was reduced 1/16 as compared to that by conventional one-layer
winding. Under .18um TSMC CMOS process the values of the equivalent circuit were listed in the following
table I. With such a small inductor and two shunted capacitors, an oscillator with high Q saw resonator at
622MHz was easily obtained. The phase noise of VCSO at 1 MHz offset is -162.5dBc/Hz. The measured
RMS jitter is 880fs and peak-to-peak jitter is 6.22ps. The tuning range was about 140 KHz. The power
consumption is 22.45mW. The clock recovery using this high quality oscillator was also studied. With the
half-rate phase detector, the oscillator was applied to high speed data rate at 1.244GBit/s.

Keyword：