Obstacle-Aware Length-Matching Bus Routing

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Abstract

As clock frequency increases, signal propagation delay on PCBs is requested to meet the timing specification with very high accuracy. Generally speaking, the net length in a single layer can estimate the routing delay in a single-layer net. In this paper, given a set of r single-layer nets in a bus with their length constraints inside mxn routing grids with s obstacle grids, based on obstacle-aware region partition inside routing grids, obstacle-aware shortest path generation and two detouring operations, R-flip and C-flip, an efficient O(mn+s3) algorithm is proposed to generate the length-matching paths for obstacle-aware bus routing. Compared with the published CAFE router, our proposed routing algorithm can save 80.5% of CPU time to complete obstacle-aware length-matching bus routing with no length error for tested examples on the average.

Keyword：PCB routing, Single-layer bus, Length-matching constraint