Post-Layout OPE-Predicted Redundant Wire Insertion for Clock Skew Minimization

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Abstract

Based on the equilibrium concept of inserting load in a physical balance, the insertion of redundant wires can be used to minimize the clock skew in an OPE-predicted clock tree. Firstly, based on the OPE prediction in lithography-based analysis and extraction, the OPE-predicted equivalent widths of all the connections in the clock tree can be determined. Different loads can be further inserted on feasible nodes in the OPE-predicted clock tree to minimize the clock skew. If the tolerant space on any tapping node is not enough for the load insertion, the inserted load on the node can be distributed into the sinks in the OPE-predicted clock tree to reduce the total load. In contrast, if the tolerant space on all the tapping nodes is enough for the load insertion, the inserted loads on the nodes can be transformed into redundant wires and the redundant wires can be routed in the routing plane. For five tested benchmarks, the experimental results show that our proposed algorithm only increases 2.8% of the total load on the average for the insertion of OPE-predicted redundant wires and decrease decreases 30.85 ps of the clock skew on the average to obtain the near zero-skew result in reasonable CPU time.

Keyword：Clock tree, Clock skew