Top-Down-Based Symmetrical Buffered Clock Routing

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Abstract

It is important for a synchronous design to minimize the clock skew in a clock tree. In this paper, based on the length-matching benefit in exact routing, an efficient four-stage algorithm is further proposed to generate a symmetrical buffered clock tree with smaller clock skew under a given slew-rate constraint. For symmetrical buffered clock routing, compared with Shih's approach, the experimental results show that our proposed approach can use extra 2.54% of total resource to reduce 85.78% of clock skew in a symmetrical buffered clock tree with satisfying the slew-rate constraint for tested benchmarks in less CPU time on the average.

Keyword：Clock routing, Buffer insertion, Skew