Efficient Assignment of Inter-Die Signals for Die-Stacking SiP Design

顏金泰,高佳涵,黃明欽,陳志瑋
Computer Science & Information Engineering
Computer Science and Informatics
yan@chu.edu.tw

Abstract

Compared with the traditional flow for IC designs, the assignment of inter-die signals is an important stage in a die-stacking SiP design. In this paper, firstly, a connection graph for all the pads in a boundary stack can be constructed and a set of dynamic tracks can be defined from the corresponding connection graph. Based on the definition of the dynamic tracks in a connection graph, a modified left-edge approach is proposed to iteratively assign the inter-die signals onto feasible pads under the constraints of the crossing and connection conditions. Compared with the published two-stage approach[5], the experimental results show that our proposed approach reduces 99% of CPU time and 0.9% of total wirelength to assign all the inter-die signals for the tested examples on the average.

Keyword：SiP design, Inter-die signal, 3D IC