Post-Layout Redundant Wire Insertion for Fixing Min-Delay Violations

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Abstract

In a complex sequential circuit, the problem of fixing min-delay violations becomes more and more important. To our knowledge, no efficient approach is proposed to eliminate the min-delay violations in a layout-level implementation. In this paper, the min-delay violations in a layout-level implementation are considered. By using the available space along the routing wires, redundant loads can be inserted into the space to increase the interconnect delay. Based on the insertion of the post-layout wires for redundant loads, a top-bottom-based insertion approach is proposed to insert post-layout redundant wires to fix the min-delay violations in a layout-level implementation. The experimental results show that our proposed approach only increases 0.84% of the total wirelength on the available space to insert post-layout redundant wires to fix 100% of the min-delay violations in a layout-level implementation for 6 tested circuits on the average in reasonable CPU time.

Keyword：Flip-flop, hold time, Setup time