Construction of Constrained Multi-Bit Flip-Flops for Clock Power Reduction

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Abstract

Based on the elimination feature of redundant inverters in merging 1-bit flip-flops into multi-bit flip-flops, given the congested constraint of unallocated bins and the length constraints of the input and output signals of all the 1-bit flip-flops, an efficient two-phase approach is proposed to obtain the final multi-bit flip-flops. Compared with the original design in the numbers of inverters for two tested examples, the experimental results show that our proposed approach eliminates 68% of inverters to maintain the synchronous designs and saves 19.75% of the clock power on the average for two tested examples in reasonable CPU time.

Keyword：clock power, Flip-flop