Low-Power Multiplier Design with Row and Column Bypassing

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Abstract

Based on the simplification of the incremental adders and half adders instead of full adders in an array multiplier, a low-power multiplier design with row and column bypassing is proposed. Compared with the row-bypassing multiplier, the column-bypassing multipliers and the 2-dimensional bypass multiplier for 20 tested examples, the experimental results show that our proposed multiplier reduces 25.7% of the power dissipation with only 15% hardware overhead on the average for 4x4, 8x8 and 16x16 multipliers.

Keyword：Low power design, Multiplier, Bypassing