Thermal Via Planning for Temperature Reduction in 3D ICs

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Abstract

In this paper, based on the temperature calculation in block-level thermal model, a two-phase approach is proposed to reduce the final floorplan temperature by redistributing the white space in all the device layers and inserting the thermal vias onto the available white space. The experimental results show that our proposed approach reduces 5.5%, 11.3% and 20.5% of temperature on 100%, 110% and 120% floorplan regions in reasonable CPU time for ten GSRC benchmarks on the average, respectively.

Keyword：3D IC, Thermal via, Temperature reduction