IO Connection Assignment and RDL Routing for Flip-Chip Designs

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Abstract

Given a set of IO buffers and a set of bump balls with the capacity constraints between two adjacent bump balls, based on the construction of the Delaunary triangulation and a Manhattan Voronoi diagram, an O(n2) assignment algorithm is proposed to assign all the IO connections in a single redistribution layer for IO connection assignment, where n is the number of bump balls in a flip-chip design. Furthermore, based on the computation of the probabilistic congestion for the assigned IO connections, an O(n2) routing algorithm is proposed to minimize the total wirelength to route all the assigned IO connections while satisfying the capacity constraints for single-layer RDL routing. Compared with the combination of a greedy IO assignment and our RDL routing, our IO assignment reduces the total wirelength by 9.9% and improves the routability by 8.8% on the average for 6 tested circuits. Compared with the combination of a greedy IO assignment, the single-layer BGA global router [Tomioka and Takahashi 2006] and our RDL detailed routing, our IO connection assignment and RDL routing reduces the total wirelength by 12.9% and improve the routability by 10.2% on the average for 6 tested circuits. Besides that the experimental results show that our IO connection assignment and RDL routing can reduce 52.1% of the total wirelength on the average to achieve 100% routability for 12 tested industrial circuits under reasonable CPU time.

Keyword：Flip-chip design, RDL routing, Single-layer routing