# Evolvable hardware design based on a novel simulated annealing in an embedded system

Guoliang He,Naixue Xiong,Laurence T. Yang,Tai-hoon Kim,許慶賢,Yuanxiang Li,Ting Hu
Computer Science & Information Engineering
Computer Science and Informatics
chh@chu.edu.tw

## Abstract

The auto-design of electronic circuits for the next generation Information Technology (IT) computing environments is currently one of the most extensively studied issues in the field of evolvable hardware (EHW) architectures. It aims to improve the reliability and fault-tolerance of hardware systems using embedded techniques. As the scalability of logic circuits becomes larger and more complex nowadays, its auto-design is more and more difficult. In order to improve the efficiency and the capability of digital circuit auto-design, in this paper, a multi-objective simulated annealing (MSA)-based increasable evolution approach is proposed in an embedded system. First, an extended matrix encoding method is used to indicate the potential performance of a circuit. Therefore, the risk of deleting a circuit with a good developing potential during evolution can be reduced. Second, we consider each output of a digital circuit as an objective, and MSA is designed for digital logic circuits with gradual evolution scheme. In the process of evolution, each objective is evolved in parallel with adaptive mechanism of neighborhood and a performance evaluation. Finally, a framework of online evolution with macro-blocks is employed to implement MSA on a field-programmable gate array efficiently and securely. In our experiments, six

arithmetic circuits are designed to assess the performance of MSA with gate-level and function-level
approaches comparing to other algorithms. The comparison results show that our method is very efficient
in the auto-design of EHW. Copyright  2010 John Wiley & Sons, Ltd.

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