Shop Floor Control Model for Wafer Fabrication and Flip Chip

杜瑩美
Industrial Management
Management
amytu@chu.edu.tw

Abstract

Semiconductor manufacturing is a capital and technology intensive high-tech industry with complex processes. As the technology evolution, to satisfy the high pin-count and performance requirements, flip-chip became the predominant technology for chip-to-next level interconnect. Due to yield concern, the tops foundries, such as TSMC & UMC, build their own package factories for flip-chip processes. However, the capacity of flip-chip factory is usually less than fabs' and becomes the bottleneck of all processes. It results in a large number of WIP, long cycle time and overdue orders and comes into being the disaster of foundry.

In this study, a shop floor control model for wafer fabrication and flip-chip factory will be developed. It includes job release policy and lot priority adjustment rule of wafer fab. Due to the variability of package technique and demand, a shop floor control model will be developed to solve current production planning and control issues. A dynamic lot priority adjustment rule will be established to apply to fab. This rule will be based on the WIP level of flip chip to dynamically adjust the lot priority in wafer fabrication stage. Therefore, the dynamic buffer management will be applied to control WIPs of fab. In this work, the lower bound and upper bound of WIP in front of constraint machine will be set and to divide the WIP level into three zones, red, yellow and green zone. When WIP level falls into red zone (less than lower bound), lot priority in wafer fabrication stage should be set higher. On the contrary, if WIP level falls into green zone (more than upper bound), lot priority can be set lower. Furthermore, DBR scheduling concept will be applied to the wafer release plan for flip-chip factory. According to the pace of the constraint machine to release wafer, it can make sure to maximize the factory throughput and to keep the WIP lower. Hence, based on these two controls, the flow will be more smooth and efficient both on wafer

fabrication and flip-chip factory.

Keyword：Wafer fabrication, Flip-chip package, Shop floor control, Dynamic buffer management, DBR scheduling